A Single-Ended Gain-Boosted Folded-Cascode Operational Transconductance Amplifier in 45-nm CMOS Technology

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"I have not failed. I've just found 10,000 ways that won't work."
— Thomas Edison

Academic Integrity Statement

I certify that this report represents my team's own original work. No prior-year designs, reports, or external unpublished materials were used. All assistance from tools such as AI is disclosed where applicable.

Contents

Abbreviations List

Acronym	Definition
AC	Alternating Current
CMRR	Common-Mode Rejection Ratio
CMOS	Complementary Metal-Oxide-Semiconductor
CD	Common-Drain
CG	Common-Gate
CM	Common-Mode
CS	Common-Source
dB	Decibel
DC	Direct Current
GBW	Gain-Bandwidth Product
IC	Integrated Circuit
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS	N-Channel Metal-Oxide-Semiconductor
OTA	Operational Transconductance Amplifier
PM	Phase Margin
PMOS	P-Channel Metal-Oxide-Semiconductor
PSRR	Power Supply Rejection Ratio
PVT	Process, Voltage, and Temperature
SR	Slew Rate
THD	Total Harmonic Distortion
VDD	Positive Supply Voltage
VSS	Negative Supply Voltage

Executive Summary

Initial Architecture: Gain-Boosted Folded-Cascode (Supplemental Design).
Our primary and most time-consuming effort focused on a single-ended, two-stage OTA architecture. The first stage was an NMOS-input folded-cascode OTA with gain-boosting. A constant-g_m bias circuit was developed to generate and mirror stable reference currents and bias voltages for the folded-cascode core. This architecture was chosen for its high intrinsic gain and wide bandwidth of a folded cascode while still supporting usable input ICMR and output swing under the 1.5 V supply constraint. NMOS inputs were selected for their higher transconductance and for placing the input common-mode closer to V_{SS}. The first-stage output common-mode was biased near mid-supply to preserve headroom for the second stage. To reach the 89 dB gain requirement, we employed differential gain-boosting (baby op-amps) that sensed small changes at the cascode node and drove the cascode gate to keep the node nearly fixed in voltage, increasing the effective r_o and overall stage gain. Simulation of this architecture demonstrated that the folded-cascode plus second stage could achieve approximately 90.2 dB low-frequency gain and a CMRR (about 95 dB) with a slew rate ($\sim 271\,\mathrm{V}/\mu\mathrm{s}$). However, the additional stages and gain-boosting loops introduced multiple non-dominant poles and zeros, making frequency compensation and phase-margin control challenging. Furthermore, the stacking of devices to support gain boosting and the second stage significantly reduced output swing and ICMR. Additionally, we did not have time to integrate the constant-g_m bias generator and CMFB network, thus the folded-cascode OTA remains an incomplete. Its schematics and limited results are included in the Appendix as documentation with lots of effort devoted.

Final Architecture: Fully Differential 5-Transistor OTA with Common-Source Stage.
On the final day of the project, following advice from Dr. Floyd, we pivoted to a much simpler topology: a fully differential NMOS-input 5-transistor OTA with a common-source second stage output. The core consists of an NMOS diff pair with PMOS loads and a tail current source driven by the previously mentioned constant Gm biasing circuit. The outputs each see only two stacked devices to the rails, which preserves voltage headroom. The common source stage, due to its simple 2 transistor design, allowed for a fully differential output swing of 1.688 volts V. A straightforward common-mode feedback (CMFB) network and simple resistive compensation (two 4.02 kΩ resistors across the outputs) were used to set the output common-mode and stabilize the loop. The main remaining shortfalls of the final design are its relatively low DC gain (~ 47 dB vs. 89 dB) and limited PSRR^+ (on the order of 40 dB versus the 120 dB specification), along with a settling time of about 100 ns. The simplified fully differential topology used the available headroom much more efficiently than the folded-cascode with a small number of stacked devices in the signal path. This allowed for a wide input common-mode range and nearly full differential output swing, while achieving the bandwidth and phase margin with compensation.

1 Compliance Table

Summary of performance versus required specifications. Specifications not met appear in red.

Specification	**Target**	**Small Fully-Diff @ 1.5 V**	**Attempted Folded-Cascode Single Ended****
Low-Frequency Gain	89 dB	47 dB	90.2 dB
GBW Product	> 120 MHz	158 MHz	31.6 MHz
Phase Margin	78°	78.2°	n/a
Output Swing ($V_{\text{pp,diff}}$)	1.6 V	1.69 V	0.593 V
Input CM Range	1 V overlap	1.03 V	0.95 V
CMRR	> 80 dB	80.2 dB	95 dB
PSRR$^+$	> 120 dB	40 dB	65 dB
Power Dissipation	< 7 mW	< 4.24 mW	n/a
Settling Time	< 90 ns	100 ns	20 ns
Slew Rate	$> 18\,\text{V}/\mu\text{s}$	$92.3\,\text{V}/\mu\text{s}$	$271\,\text{V}/\mu\text{s}$
Input-Referred Noise	$< 14\,\text{nV}/\sqrt{\text{Hz}}$	$10\,\text{nV}/\sqrt{\text{Hz}}$	$4.68\,\mu\text{V}/\sqrt{\text{Hz}}$
Wide Bandwidth	> 120 MHz	706 kHz	1 MHz

Table 1: Compliance table for nominal simulated performance.

**Note: DC biasing was used for this supplementary circuit with $V_{\text{biasN}} = 0.6$ V, $V_{\text{biasP}} = 1$ V, $V_{\text{optN}} = 1.05$ V, and $V_{\text{optP}} = 0.3$ V. This circuit is provided as supplemental information to demonstrate the immense effort and time that my partner and I devoted to this project. Not all results are included as they were generated last minute as evidence of our work on an incomplete and more complex OTA.

2 Roles and Work Distribution

This project was completed by Payton Domville and John Goebel. We worked together on all major decisions and agree that the overall effort is approximately a 50/50 split.

Table 2: Summary of roles and work distribution.

Design / Task Area	**Payton Domville**	**John Goebel**
Overall architecture and specs interpretation	Shared	Shared
Device characterization	Shared	Shared
Differential OTA core and gain boosting	Shared	Shared
Bias generator and bias tree	Lead	Support
CMFB and attempted startup circuitry	Lead	Support
Second stage and output buffer	Shared	Shared
Testbenches (gain, GBW, PM, CMRR, PSRR, swing, etc.)	Support	Lead
Noise and Monte Carlo verification	Shared	Shared
Cadence library setup / maintenance	Shared	Shared
LaTeX report writing and figures	Shared	Shared

Both authors reviewed the schematics, simulations, and report, and are in agreement.

3 Technical Discussion

3.1 Use of AI Tools

OpenAI's ChatGPT and Google's Gemini AI tools were used throughout the entirety of the project. They assisted in the initial stages of planning/debating circuit architectures and topologies against the required specifications, literature searches on folded-cascode OTA fundamentals (with Open AI's Deep Research tool), circuit debugging and design methodology, back-of-the-envelope calculation verification for saturation regions circuits (such as the folded-cascode topology), biasing and transistor sizing strategies to avoid circular reasoning, Cadence/Linux error message debugging and solutions in FastX4, Latex formatting of the design report, and other related topics. Specific prompts for the project included, and are not limited to, questions similar to the following list: How do you check the power consumption of a circuit in Cadence; Describe a design approach for gain-boosting amplifiers for the NMOS and PMOS cascodes in a folded-cascode OTA to increase differential gain; Explain the principle of fully differential common-mode feedback loop for a folded cascode OTA such that it maintains the output common mode level; For a folded-cascode OTA architecture, what are reasonable back-of-the envelope values for the VoptN, VoptP, VbiasN, and VbiasP voltages in 45-nm CMOS technology; Explain to me the general differences with process length-variation and saturation regions for CMOS transistors; In ADE Explorer, how do I configure a parametric analysis such that I can sweep a design variable and automatically generate my DC and AC curves; Given that we are working with 45-nm technology, what is a reasonable or the most common design length for this process in analog design; How do you run a Monte Carlo Simulation within ADE Explorer; What are the conceptual trade offs between single wide-swing diode connected devices or one with two diode connected devices for a folded cascode OTA core; In the early stages of folded-cascode design, is it reasonable to set the same channel length for all the transistors; Should I first choose transistor widths and lengths for each device group in the folded cascode OTA and then adjust the bias currents or is it better to start from targeted currents and Veff values and then solve for W's; Is there a way in Cadence to change the channel length of every transistor in my schematic at once instead of editing them individually; How can I edit the associated schematic of a symbol within a test bench file for an ADE Explorer simulation; Is a start-up circuit for a operational transconductance amplifier absolutely necessary for simulation purposes; etc. The exhaustive list of specific queries, for all stages of the workflow, and as a search engine tool goes on and on, but their details are irrelevant in indicating the use of AI in this project. The AI tools were largely used as a resource for circuit design, conceptualization, theory, and cadence implementation support. That being said, all final architecture design, devices sizing methodologies, simulations, biasing choices, and conceptual circuit work is original to the authors. Additionally, AI was used for textual grammar edits and revisions for clarity in the report.

3.2 OTA Architecture Overview

We first chose to design a folded-cascode OTA. The standard cascode increases gain by boosting output impedance while keeping roughly the same g_m as a simple CS stage. This general theme of higher output impedance is beneficial for higher gain applications.

Stacking can be extended by adding additional CG stages to further increase output impedance by a factor of u_f per device. This comes at the cost of burning extra V_{DS} headroom to keep all transistors in saturation. A telescopic cascode core was initially considered for higher intrinsic gain, but in 45-nm CMOS at 1.5 V it produced a very narrow and impractical input CM range with small output swing. In contrast, the folded cascode applies the same idea of raising the output impedance but splits the loading into two branches using complementary PMOS and NMOS folding devices. This allows the input pair to sit one device away from V_{DD} or V_{SS} while still presenting a high-impedance output node.

Moving from a telescopic to a folded-cascode architecture reduces intrinsic gain and shifts secondary poles, but it increases output swing, widens input CM range, and offers more headroom flexibility under the 1.5 V supply constraint. Our design used an NMOS input pair for better g_m per unit current and to place the input CM closer to V_{SS}. In practice, biasing the upper PMOS and lower NMOS devices so they stayed in saturation across the CM sweep was difficult. We were constantly trading off between keeping devices safely in saturation and not wasting headroom, which directly affected maximum output swing.

Meeting all specifications was challenging. While the folded-cascode topology provided the needed headroom, achieving both low-frequency gain > 89 dB and GBW > 120 MHz required gain-boosting auxiliary amplifiers. These "baby" op-amps around the cascode devices significantly complicated the circuit's pole pattern. Attempts to push non-dominant poles to higher frequencies often conflicted with the CMRR requirement and forced us to resize PMOS loads and adjust currents. Increasing gain by raising output impedance tended to pull the non-dominant poles down, making the 78° phase-margin target difficult to hit.

Given these complexities and headroom limitations, we ultimately pivoted to a much simpler final topology: a fully differential NMOS-input five-transistor OTA with a common-source style output structure. This amplifier consists of an NMOS differential pair with PMOS active loads, a tail current source biased from the constant-g_m network, and a basic CMFB loop that regulates the average output voltage. Each output sees only two stacked devices to the rails, which greatly relaxes headroom constraints at 1.5 V and enables a large differential output swing. The reduced number of high-impedance nodes yields a much simpler pole structure, making stability and compensation straightforward. Although this architecture sacrifices the ambitious > 89 dB gain target, it uses the available headroom efficiently and performs well in terms of GBW, phase margin, common-mode range, output swing, and slew rate.

3.3 Transistor Sizing and Biasing Strategy

Our methodology for biasing and transistor sizing began with an ideal, systematic approach, but as the design evolved (or should I say devolved) beyond the basic folded-cascode core it quickly degraded toward a non-effective, yet intuitive mindset of making minor tweaks to test hypotheses. Initially, we characterized the 45 nm NMOS and PMOS devices in Cadence to extract key small-signal and process parameters, obtaining $V_{T,\mathrm{n}} \approx 0.48\,\mathrm{V}$, $\mu_n C_{\mathrm{ox}} \approx 234\,\mu\mathrm{A/V}^2$, $V_{\mathrm{LIN,n}} \approx 0.64\,\mathrm{V}$, $(\lambda L)_{\mathrm{n}} \approx 0.039$, $V_{T,\mathrm{p}} \approx 0.42\,\mathrm{V}$, $\mu_p C_{\mathrm{ox}} \approx 219\,\mu\mathrm{A/V}^2$, $V_{\mathrm{LIN,p}} \approx 0.59\,\mathrm{V}$, and $(\lambda L)_{\mathrm{p}} \approx 0.038$. These values provided the starting point for choosing overdrive voltages, device lengths, and bias currents in the folded-cascode OTA.

In concordance with these design values, we constructed an Excel spreadsheet to model the core of the folded-cascode OTA. The sheet utilized device parameters, including effective voltage (V_{eff}) and currents, to calculate the transistor widths required to achieve target performance. We also computed relevant small-signal parameters such as g_m, g_{ds}, g'', r_o, and u_f. By utilizing these parameters to solve for the differential-mode gain (A_{dm}) and common-mode gain (A_{cm}), we determined the ideal widths to meet the desired specifications.

For the folded cascode, we used a model that included a tail current (I_{tail}) in which a current of $I_{\mathrm{tail}}/2$ went down the input nodes. Consequently, a current of $I_{\mathrm{tail}} + I_{\mathrm{idle}}$ was supplied to the folded legs, resulting in $I_{\mathrm{idle}} + I_{\mathrm{tail}}/2$ flowing down the output legs. If we ensured that $I_{\mathrm{idle}} > 0$, the current would flow in the output legs and they would not be starved. We experimented with different ratios of I_{tail} vs I_{idle} and initially settled on a ratio of $I_{\mathrm{idle}} \approx I_{\mathrm{tail}}/2$. The methodology followed the idea that if we needed more overdrive voltage on the folded devices, we would increase the idle current to push them further away from the triode region. Increasing the current for these upper PMOS cascode devices was also pivotal in adjusting the associated g_m and the V_{DS} drop for the devices below the pair, as well as increasing the input common mode range. On the contrary, we made I_{idle} less than $I_{\mathrm{tail}}/2$ when we were trying to increase our bandwidth.

Following the ideal guidance from the hand calculations, it was an expected disappointment when we saw that the rough hand calculations did not match up with the Cadence simulation results. It was here where we continued trying to optimize the devices such that we were designing for an ideal current or V_{eff}. Further optimization for certain parameters such as input common mode range and Gain-Bandwidth product further deviated from the systematic and planned approach for device widths. In terms of headroom, we continued to follow a methodology that included placing the devices on the output stack comfortably in saturation ($\approx 300\,\mathrm{mV}$) so as not to fall into the linear/triode region.

The initial biasing followed very basic and ideal operational DC voltages that were derived with hand calculations for the folded-cascode core. While changing the biases within Cadence, we followed the commonly mentioned "sources follow gates" scheme and incrementally tuned the biases

in what felt like guesswork at times. The use of the parametric sweep for the biases proved to be very effective, where we would sweep a bias voltage within an expected range and output voltage vs. frequency plots to evaluate biasing conditions. Ideally, we attempted to bias the transistors such that they biased in saturation with a safety threshold that ranged anywhere between $50 - 100\,\text{mV}$.

When the circuit progressed to include the baby op-amp boosters, the initial transistor sizing and guidance document for currents and ideal effective voltages (V_{eff}) became pretty much irrelevant. The need to keep the boosters in saturation, along with their control of the cascode gates via feedback, created a sensitive dependency loop. We found that small changes in the booster bias would push the main cascode devices in or out of their optimal operating region. The process by which the bias voltages, ($V_{\text{opt}N}$) and ($V_{\text{opt}P}$) were determined, followed the parametrized sweep method mentioned previously.

To generate repeatable bias currents, we implemented a constant-g_m biasing circuit. A PMOS transistor with source degeneration is biased in feedback so that its small-signal transconductance is $g_m \approx 1/R_{\text{set}}$. The resulting drain current is mirrored to the OTA tail source, folded branches, and baby op-amps (Note the body of this transistor is tied to its source to eliminate any body effect). The same structure provides the node voltages labeled V_{biasN}, V_{biasP}, V_{optN}, and V_{optP} for the cascode gates. It was later reused to set the tail current in the final fully differential OTA.

3.4 Gain Boosters / Second Stage

We had trouble increasing the core OTA low-frequency gain beyond 55 dB but still had plenty of bandwidth to work with, as it extended beyond 1 GHz. Thus, we sought to employ a second stage to meet the 89 dB requirement. The second stage consists of a PMOS-input common-source stage followed by an NMOS common-gate load. The choice of a PMOS input device over an NMOS stemmed from headroom and swing considerations at the available 1.5 V supply. Given that the first-stage output common-mode sat near mid-supply $\approx 0.7\,\text{V}$, an NMOS input device would have insufficient V_{DS} headroom and would restrict the positive output swing. Whereas the PMOS input better fits the bias point and preserves output swing toward V_{DD}. The hope was that the input common mode range requirement of $> 7\,\text{V}$ overlap with the output signals would help be met with this stage on a 1.5 V supply. However, even with the second stage, it was very difficult with our understanding and design methodology to move this stage beyond an additional 20 dB to meet the 89 dB requirement while preserving bandwidth.

Given the marginal increase in DC gain, the second stage also introduced another dominant pole. This pole in combination with the poles from the first stage led to greater than intended complexity and proved to be extremely difficult in handling with frequency compensation to achieve 75° the phase margin. When compensating for the phase margin, we found that this also reduced our bandwidth, which was not ideal for achieving the optional specification. The second stage also added further power consumption, detracting from the $< 7\,\text{mW}$ power requirement, and introduced

additional noise within the output signal path. It also tightened our output-swing limits as the extra PMOS gain device and its NMOS load both have to stay in saturation. The debate for keeping the second stage with its many drawbacks and complexities for the subtle increase in gain is unresolved within our group.

After our methods of resizing and biasing proved insufficient to raise the gain of the folded-cascode core, we looked for other alternatives. Ultimately we turned to gain-boosting auxiliary amplifier (baby op-amp), topologies. The baby op-amps work by sensing small V_{DS} variations in the cascode device's V_{DS} relative to an input bias/reference voltage. They then drive the cascode gate such that its source node remains almost constant at a set DC level. Overall, local feedback this raises the effective output r_o of the cascode branch and therefore boosts the overall DC gain of the folded-cascode stage. However, this output impedance enhancement only holds over the bandwidth of the baby op-amp, and thus the additional poles and can limit the overall bandwidth of the folded cascode.

The first realization used a simple CS amplifier with a PMOS active load as the gain-boosting stage. This topology worked great for boosting gain exceeding $> 105\,\text{dB}$ but imposed significant headroom drawbacks to support the devices. Because the sensing transistor of each baby op-amp was placed in series with the cascode branch, it had to maintain a minimum $V_{DS,\text{sat}}$ (or V_{GS}) in addition to the overdrives of the folded-cascode devices. This large consumption of headroom on both the upper PMOS cascodes and lower NMOS cascodes decreased the margin for the internal node voltages and subsequently diminished our input common-mode range to values $< 300\,\text{mV}$. Therefore we moved to a gate-sensed differential baby op-amp, in which the negative input monitors the cascode node and the positive input is tied to a bias reference. In this configuration the sense node only drives a high-impedance gate, so the auxiliary amplifier no longer adds series headroom in the cascode stack, while still providing strong feedback around the cascode device through a differential bias.

3.5 Frequency Compensation

To address stability concerns within the feedback loops, we implemented a standard Miller compensation strategy. We established a baseline compensation capacitor value of $C_c = 0.5\,\text{pF}$; this value was chosen as a preliminary trade off between stability and bandwidth. To counteract the Right-Half Plane (RHP) zero introduced by the feedforward path through C_c, we placed a resistor in series with the capacitor. This resistor was sized to be slightly larger than the intrinsic $1/g_m$ value of the gain stage to push the zero to a higher frequency.

Optimization involved a parameterized analysis of the resistor value with pole-splitting theory. By tuning this resistance, we aimed to separate the poles further pushing the non dominant output pole to a higher frequency while establishing a clear dominant pole at a lower frequency thereby maximizing the phase margin for the closed loop response.

3.6 Monte Carlo Analysis Interpretation

The Monte Carlo analysis indicates that the final fully differential OTA is pretty robust. Phase margin with a standard deviation of $\approx 1.7°$, so all samples remain comfortably stable. The unity-gain bandwidth has a mean of about 158 MHz with a standard deviation of ≈ 10.8 MHz, keeping even worst-case runs above the 120 MHz requirement. The low-frequency gain also shows very little spread, with a mean of ≈ 47.3 dB and a standard deviation of only 0.63 dB. Although the nominal gain does not meet the 89 dB specification, it is pretty robust against device variation.

3.7 Optional Specification

We were given the choice between prioritizing wide bandwidth with unity-gain frequency > 800 MHz, rail-to-rail operation with CM input range of 0 to 1.5 V, low-noise performance with an input-referred noise floor $> 4\,\text{nV}/\sqrt{\text{Hz}}$, or low-power operation with total power dissipation < 1 mW. With our decision to design a folded-cascode topology, its naturally large bandwidth made the specification of > 800 MHz compelling to target. On the other hand, the rail-to-rail operation with CM input range of 0 to 1.5 V was not feasible with our current design and would require the execution of an entirely different rail-to-rail folded cascode topology, with one set of NMOS and PMOS inputs. Additionally, the low-noise performance with $> 4\,\text{nV}/\sqrt{\text{Hz}}$ and low-power operation with total power dissipation < 1 mW were briefly considered as attainable targets until the addition of gain-boosting stages within the folded cascode. Between attempting to balance the stability/bandwidth of the feedback loop for the gain-boosting stages and limiting their total power consumption, it was clear that the most feasible specification was the wide bandwidth with unity-gain frequency > 800 MHz.

First, for the folded-cascode OTA core we attempted to maximize the input-stage transconductance g_m by biasing the NMOS input devices of the folded-cascode with sufficient V_{DS} and branch current. We found that using relatively small widths for the cascode devices that were connected to the output node helped to push the unity-gain frequency above 800 MHz. However this change also constrained the designed current ratios in the output branches. Without gain boosting, this bandwidth metric was easy to meet and the difficulties arose when the gain-boosting loops were applied. While trying to reach the required DC gain without over-boosting, we saw that with excessive output-resistance enhancement from the boosting and shifted the dominant pole to much lower frequencies. The large > 105 dB gains degraded both the bandwidth and the phase margin. This is because the output-impedance enhancement from each baby op-amp is only effective over the frequency range where its own loop gain is high this limited internal bandwidth of the auxiliary amplifiers (with gain beginning to roll off beyond ~ 100 MHz).

For the common-source second stage, this further limited the achievable unity-gain frequency. While it provided the extra $20 - 30$ dB DC gain needed to meet the 89 dB requirement, the extra high-

impedance node introduced a second low-frequency pole. This required Miller compensation between the stages. This resulted in shifting the dominant-pole to a lower value along with the already finite bandwidth of the gain-boosting loops. Overall this significantly reduced the overall gain–bandwidth product and made it much more difficult to maintain $f_{\mathrm{UG}} > 800\,\mathrm{MHz}$ with adequate phase margin. This metric because increasing more complex and unattainable for the more complexity and stages that were added to the circuit.

For our fully differential amplifier, our bandwidth was was only $\approx 500\,\mathrm{kHz}$. Due to the last second design of this amplifier, we did not have time to optimize for this metric.

3.8 Performance Summary

The fully differential OTA at 1.5 V partially meets the design targets. It achieves a GBW of 158 dB, adequate phase margin, good output swing, good input CM range, CMRR of 80.2 dB, and low power dissipation (4.24 mW, and a slew rate of $92.3\,\mathrm{V}/\mu\mathrm{s}$. However, its low-frequency gain (47 dB), PSRR (40 dB), settling time (100 ns), input-referred noise, and bandwidth (706 kHz) fall short of the specifications. The attempted single-ended folded-cascode OTA achieves high gain and good CMRR/PSRR, but resulted in a low output swing, low common-mode range, and bad bandwidth with the headroom constraints.

4 Fully Differential OTA Associated Schematics (Design Values)

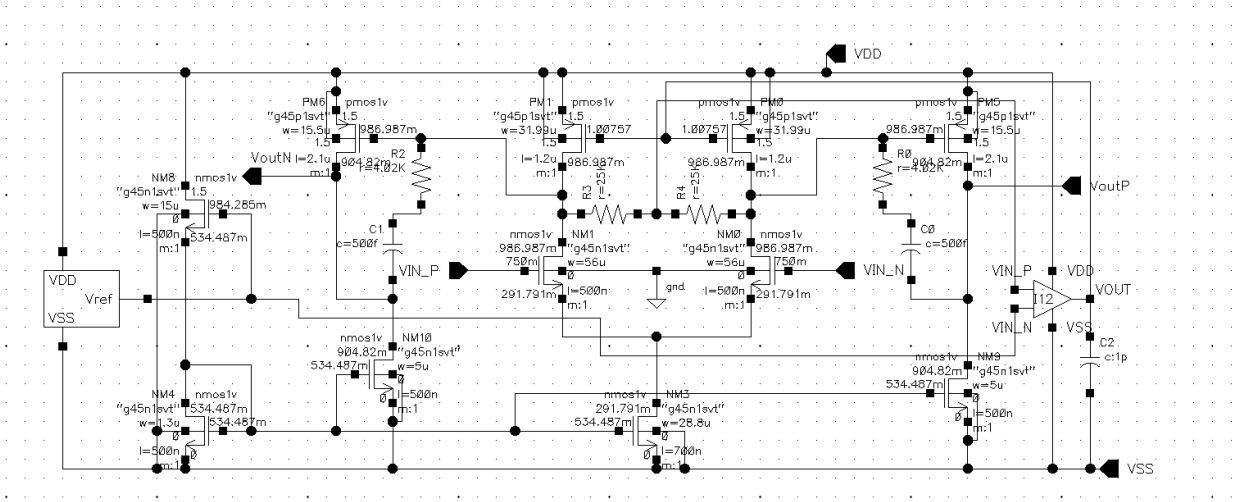

Figure 1: Schematic of the OTA core for the fully differential amplifier.

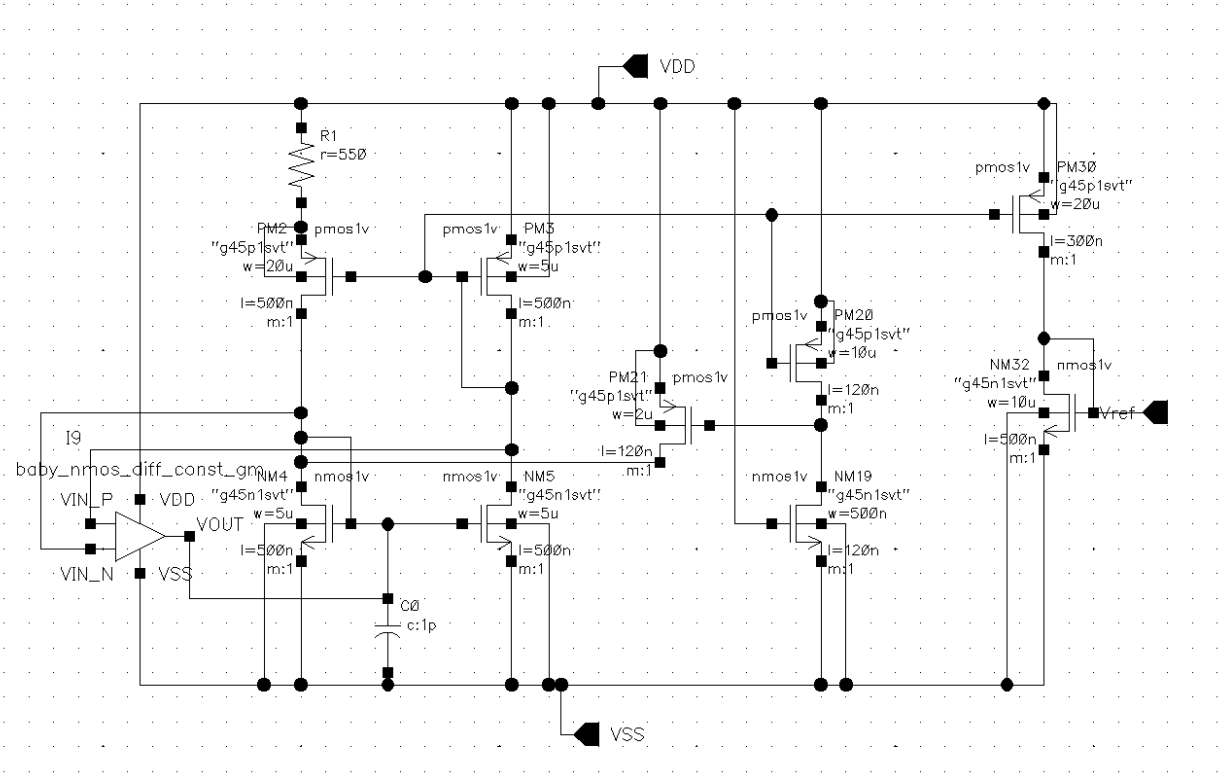

Figure 2: Constant-g_m Bias Circuit for the fully differential OTA

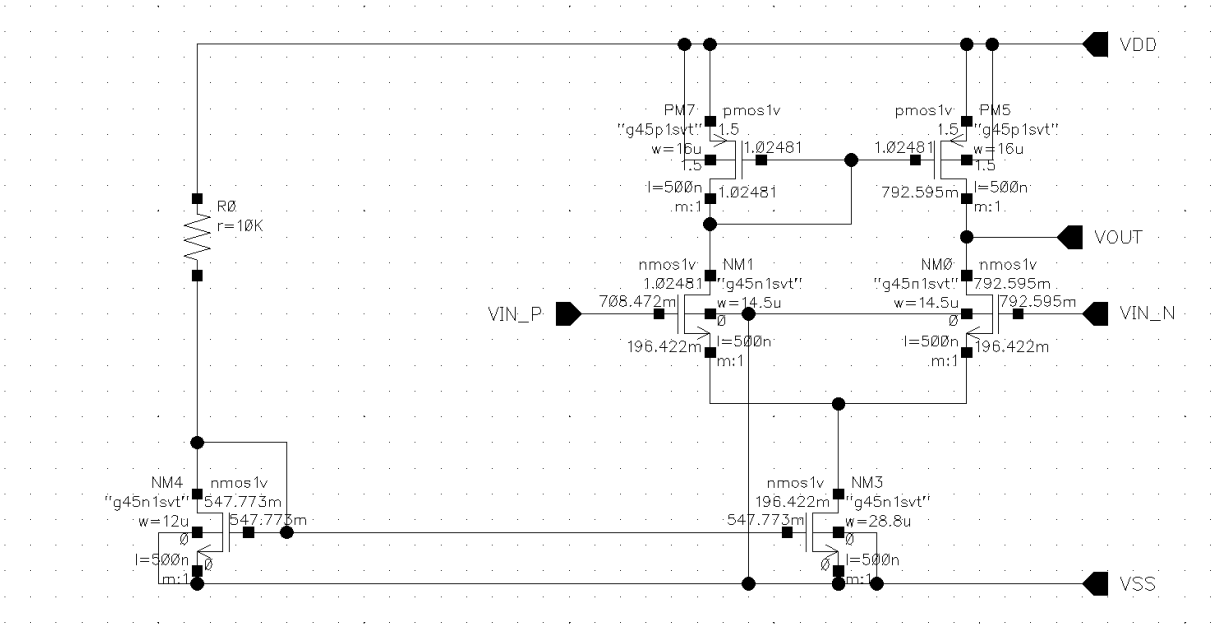

Figure 3: Baby NMOS Differential Amplifier for the Constant-g_m Bias Circuit

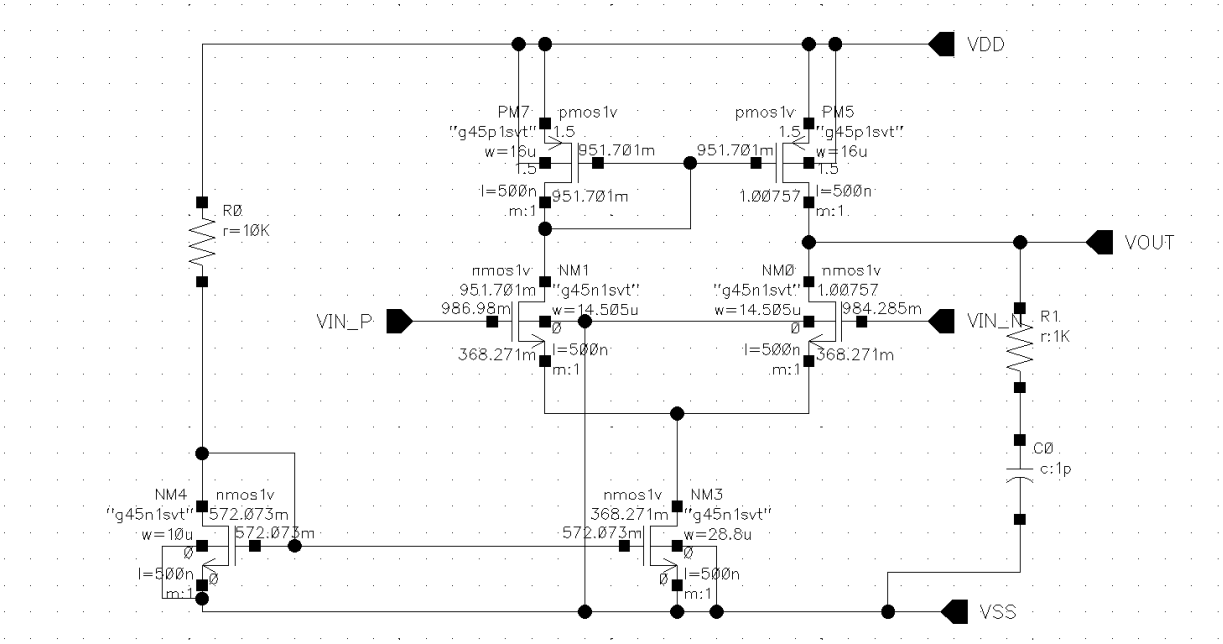

Figure 4: Baby NMOS Differential Amplifier for the common mode feedback of the OTA core.

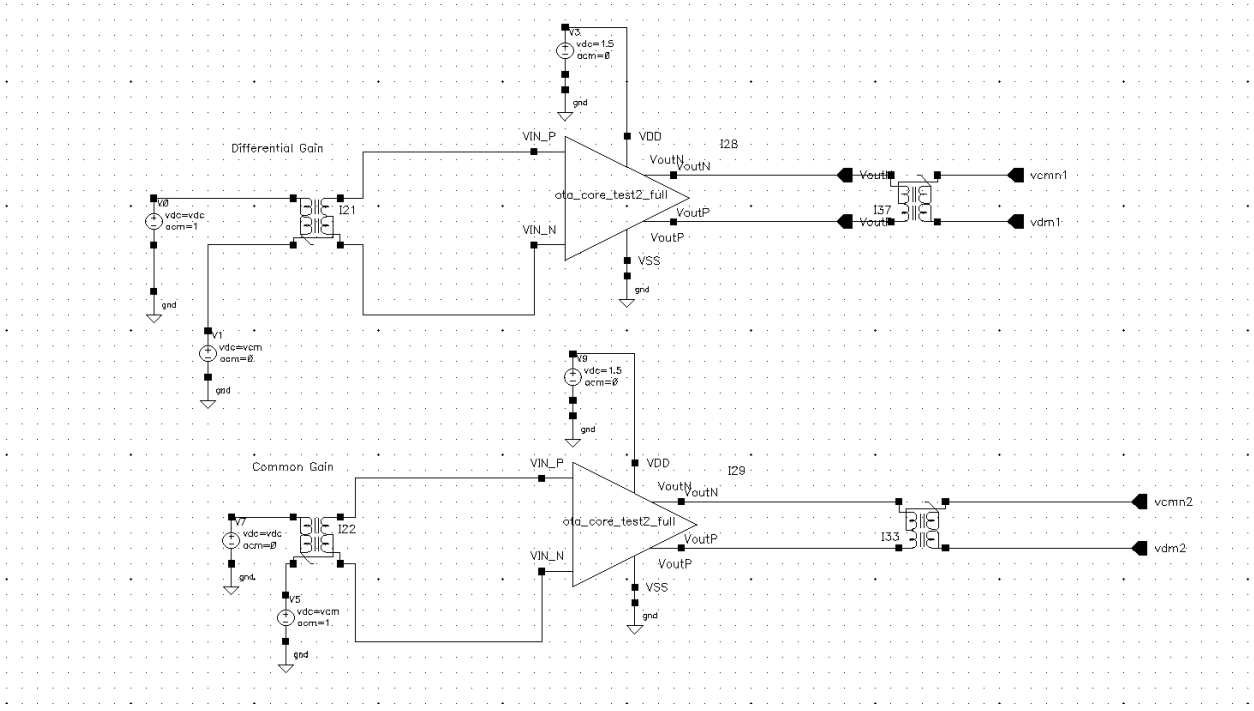

Figure 5: Test Bench schematic with DC biasing for evaluating Common Mode and Differential Mode Gains.

5 Fully Differential Amplifier Simulation Results

5.1 Frequency Response

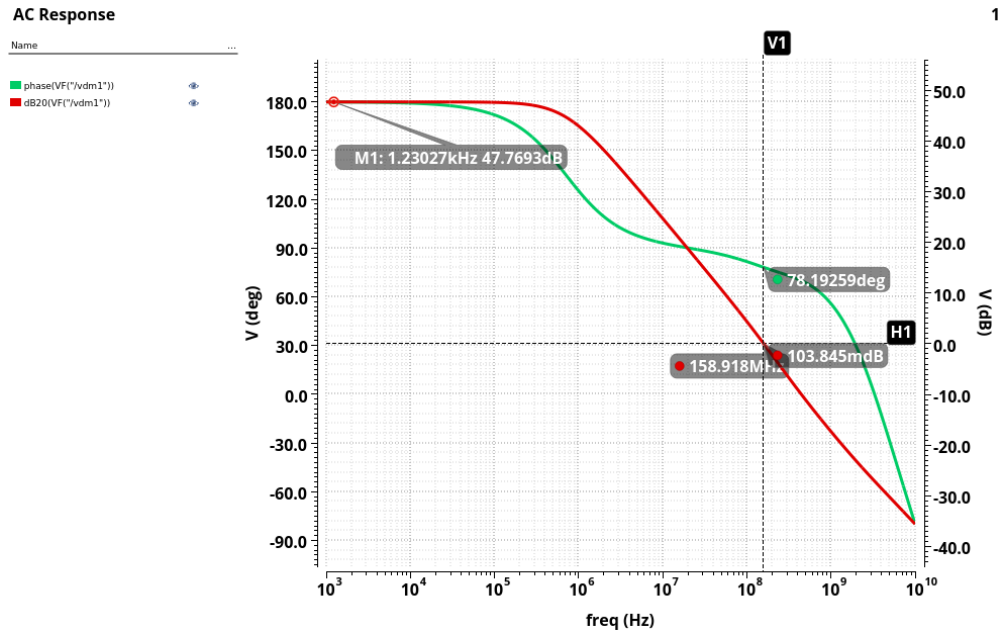

Figure 6: The phase margin for the full differential amplifier at the differential output node was compensated with two 4.02k ohm resistors to achieve a 78.2 degree phase margin. The low frequency gain is approximately 47dB.

5.2 Monte Carlo Phase Histogram

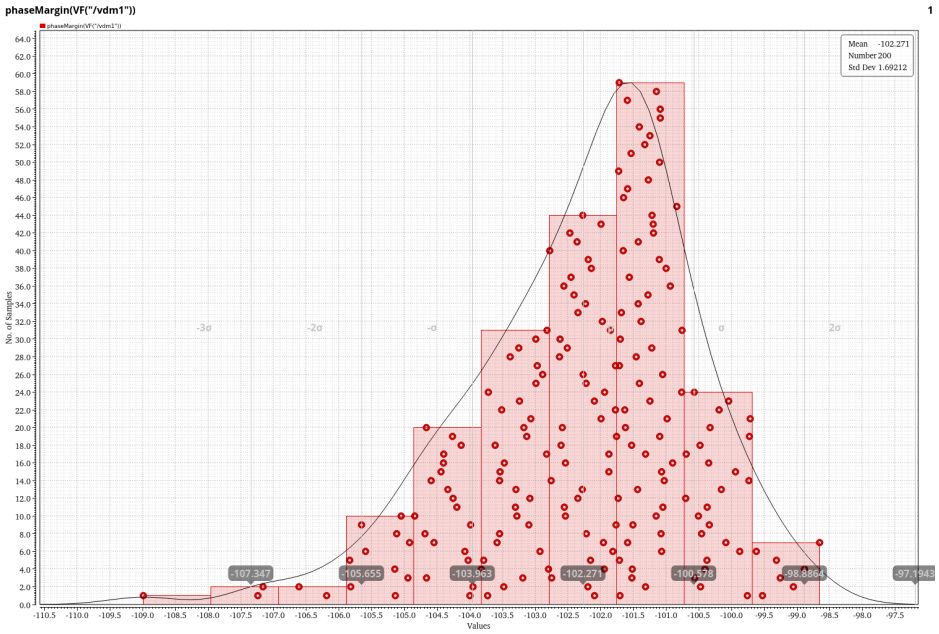

Figure 7: Monte Carlo distribution of AC gain (200 runs).

5.3 Monte Carlo GBW Histogram

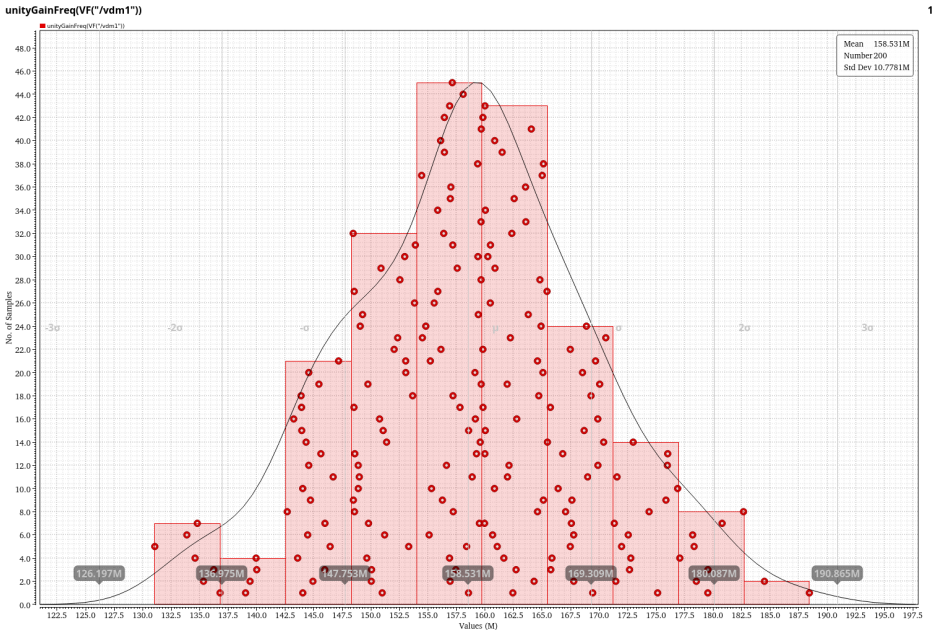

Figure 8: Monte Carlo distribution of GBW (200 runs).

5.4 Monte Carlo ADM Histograms

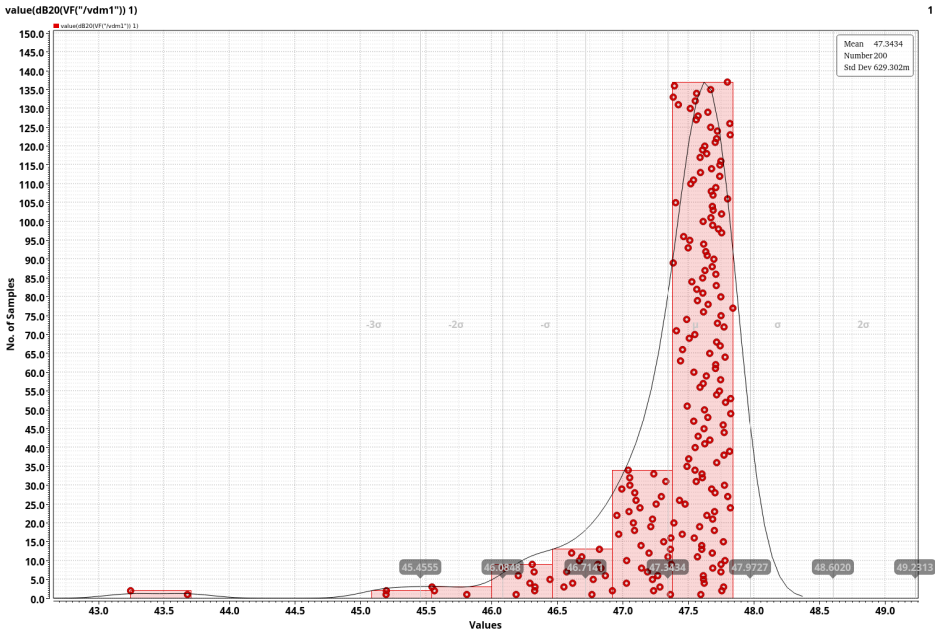

Figure 9: Monte Carlo distribution of phase (200 runs).

5.5 Step Response / Settling Time

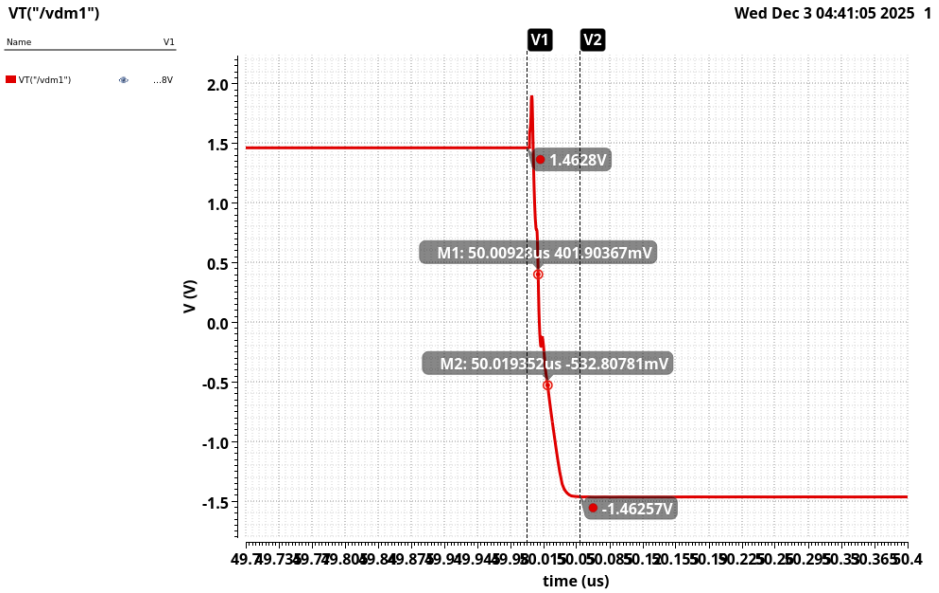

Figure 10: The slew rate is approximately 92.3 V/μs, and the response time is approximately 100 ns.

5.6 DC Input Range

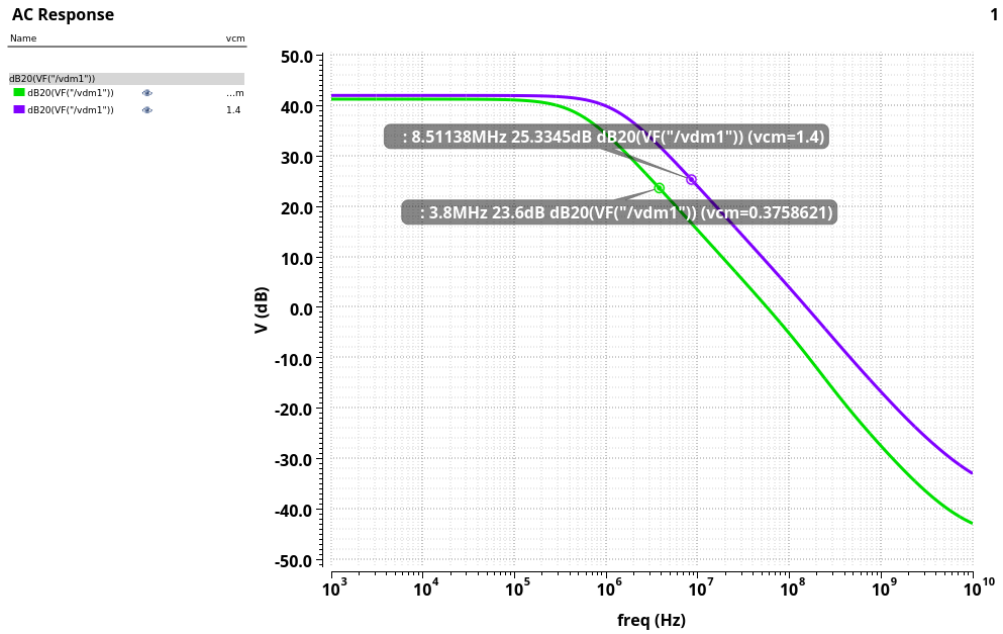

Figure 11: The DC input range is approximately 1.03 V.

5.7 Output Range

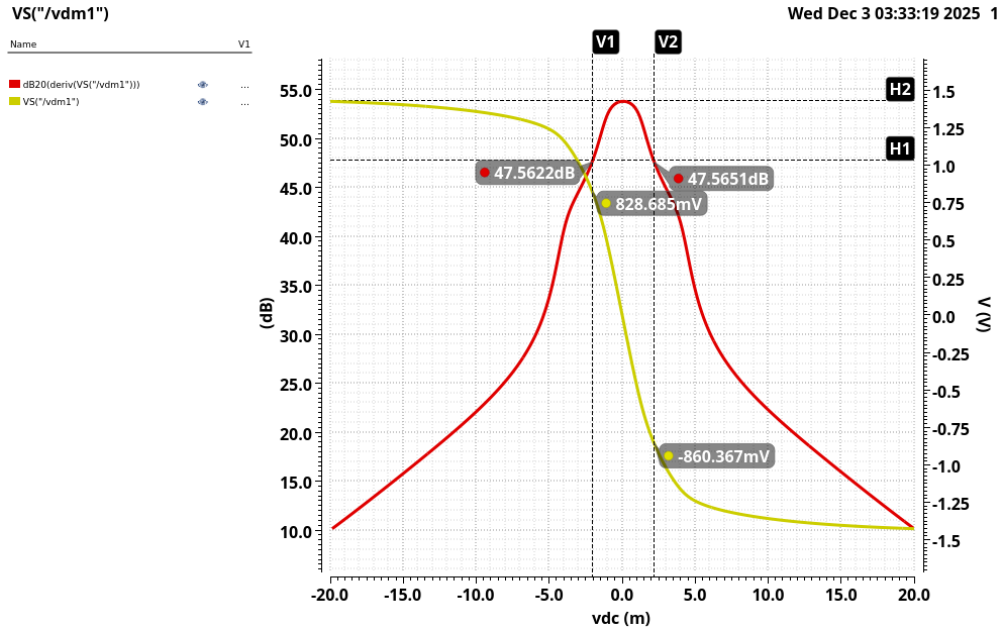

Figure 12: The output range is approximately 1.688 V.

5.8 CMRR

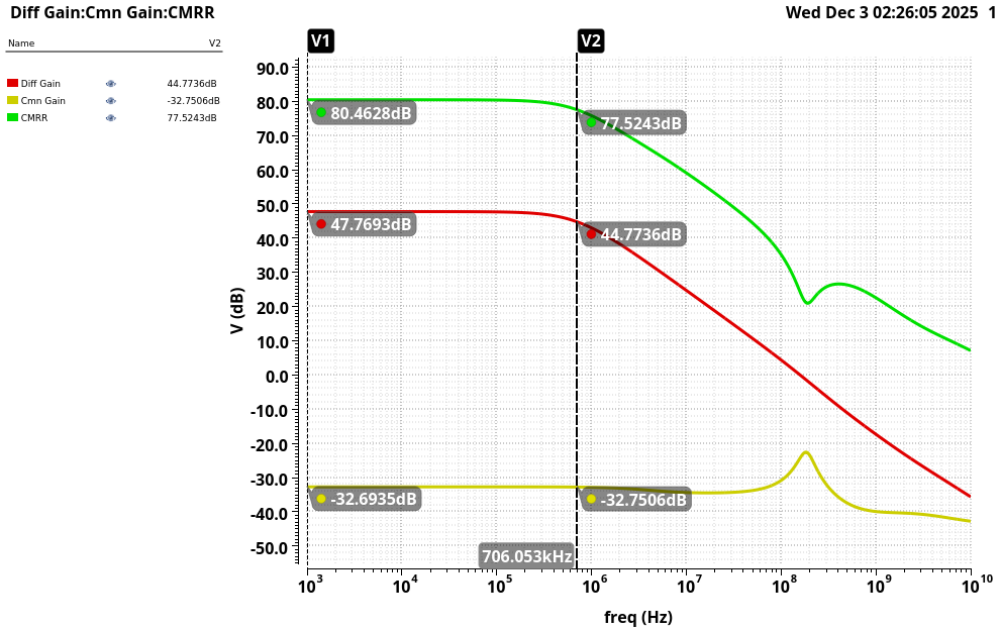

Figure 13: The common-mode rejection ratio (CMRR) is approximately 80.42 dB.

5.9 PSRR

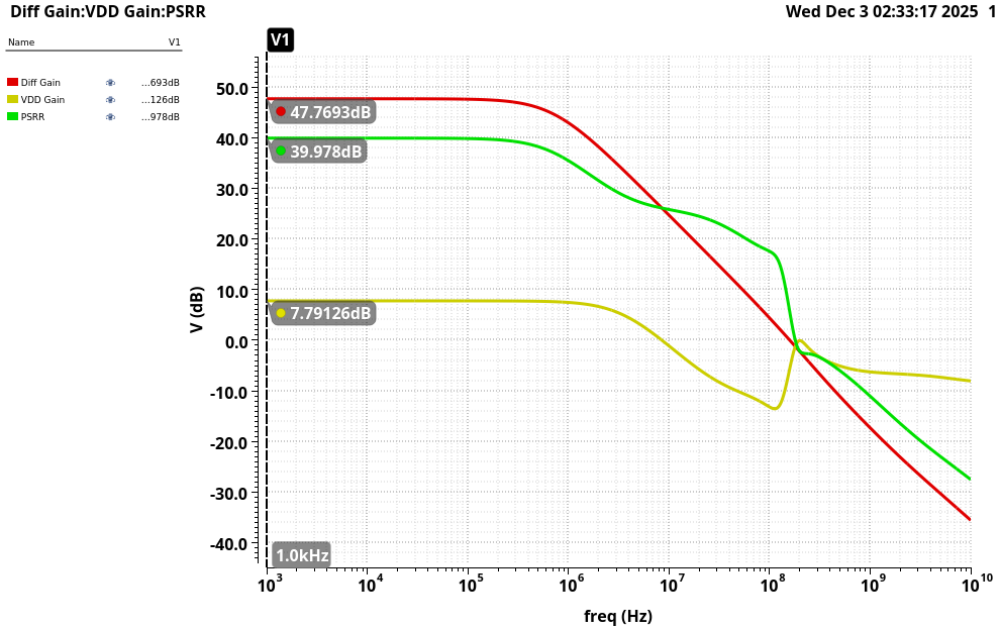

Figure 14: The power-supply rejection ratio (PSRR) for the fully differential amplifier is approximately 40 dB.

5.10 Input-Referred Noise

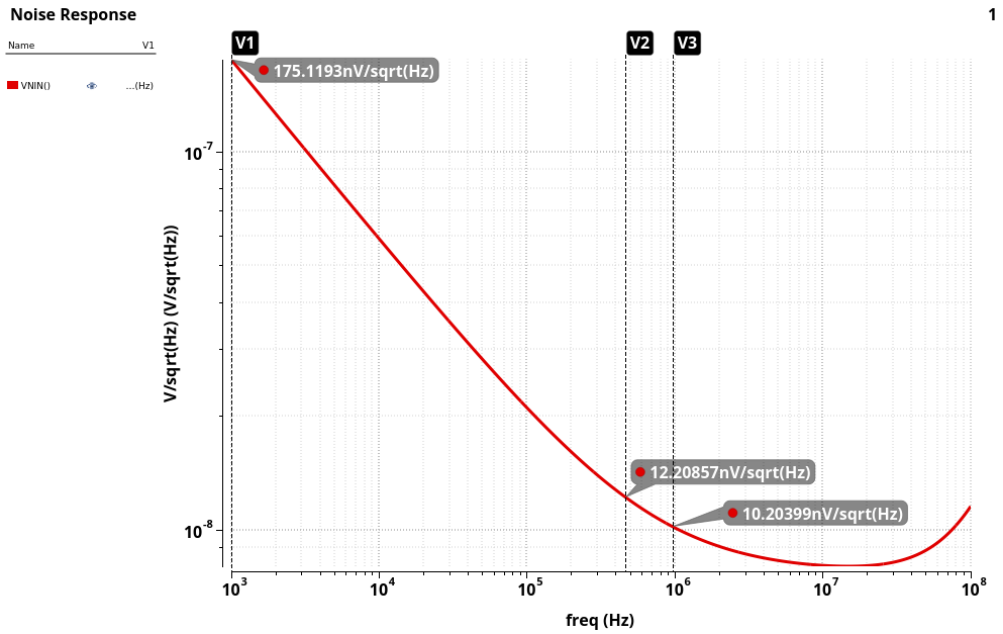

Figure 15: The noise level after the $1/f$ corner is approximately $10\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$.

5.11 Input-Referred Noise Metrics

Device	Param	Noise Contribution	% Of Total
/I28/R4	rn	0.000146449	0.12
/I29/R3	rn	0.000146449	0.12
/I29/R4	rn	0.000146449	0.12
/I28/R3	rn	0.000146449	0.12
I29.NM1.xrg.r1	thermal_noise	0.000131712	0.10
I29.NM0.xrg.r1	thermal_noise	0.000131712	0.10
I28.NM1.xrg.r1	thermal_noise	0.000131712	0.10
I28.NM0.xrg.r1	thermal_noise	0.000131712	0.10
I29.PM1.xrg.r1	thermal_noise	6.67242e-05	0.02
I29.PM0.xrg.r1	thermal_noise	6.67242e-05	0.02
I28.PM1.xrg.r1	thermal_noise	6.67242e-05	0.02
I28.PM0.xrg.r1	thermal_noise	6.67242e-05	0.02
/I28/R2	rn	3.82266e-05	0.01
/I28/R0	rn	3.82266e-05	0.01
/I29/R2	rn	3.82266e-05	0.01
/I29/R0	rn	3.82266e-05	0.01
I29.NM10.xrg.r1	thermal_noise	1.73095e-05	0.00
I29.NM9.xrg.r1	thermal_noise	1.73095e-05	0.00
I28.NM10.xrg.r1	thermal_noise	1.73095e-05	0.00
I28.NM9.xrg.r1	thermal_noise	1.73095e-05	0.00

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.00426831
Total Input Referred Noise = 9.41938e-05
The above noise summary info is for noise data

Figure 16: Input-Referred Noise Metrics for the Fully Differential Amplifier.

6 Conclusion/Reflection

Overall, this project was a tremendous learning experience with what felt like an exponential learning curve. As my partner and I did not have any experience with Cadence circuit design before this class, so this was a significant step up. Retrospectively, I believe our ambition got the best of us. Instead of sticking with the fundamentals, we consistently tried to tackle our circuit's flaws with more complex circuitry rather than addressing the core issues.

In terms of the major events, we initially began with a very simple NMOS single-ended amplifier that worked well. This stage served as a "warm up" where we successfully set up our test benches. We then progressed to the folded cascode. After maxing out the gain at around 55 dB, we added a second stage in hopes of achieving more gain. The second stage added around 20 dB, but this was still short of our goals. In hindsight, we were almost entirely fixed on gain and bandwidth, losing sight of the other performance metrics we were targeting.

We then added the "baby op-amps" for gain boosting, trying several variations including a simple Common-Source with active load and a differential amplifier. This is where we started to get ahead of ourselves, getting stuck in a cycle of optimizing these auxiliary amps in conjunction with the folded cascode. Overall, we did successfully implement the architecture to hit the low-frequency gain and bandwidth requirements, but this came at the cost of many other metrics and a significant amount of time.

At the last minute, and with Dr. Floyd's advice, we returned to a very simple differential amplifier model to try and hit as many parameters as we could. Finally, regarding our tools, the master Excel sheet worked very well for the earlier stages and for understanding the fundamentals of the folded cascode, but it became less effective during the later stages of complex circuit design.

We are completing this now, putting the final touches on our report as the sun rises...

Appendix

A Fully Differential OTA Associated Schematics (Operating Points)

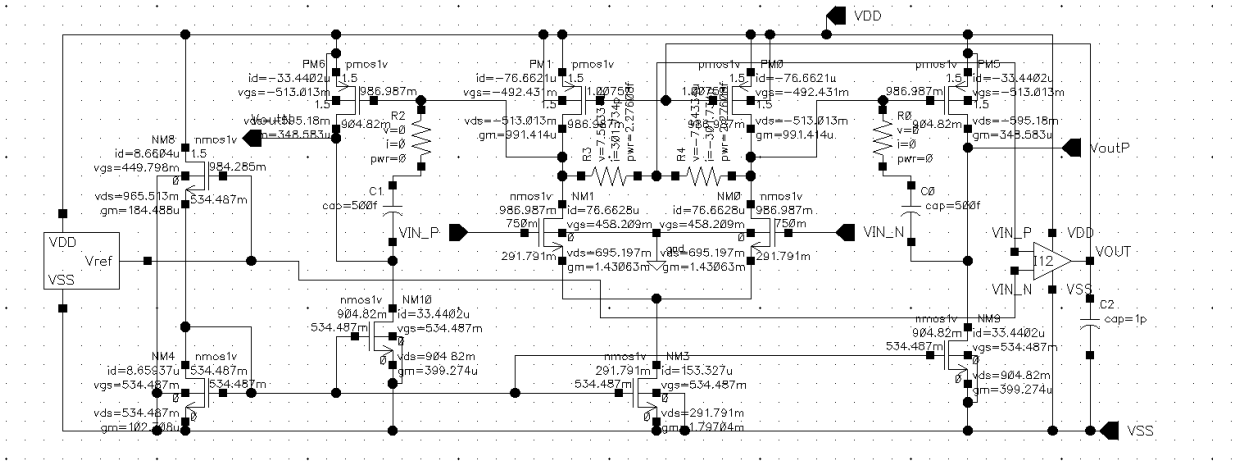

Figure 17: Schematic of the OTA core for the fully differential amplifier.

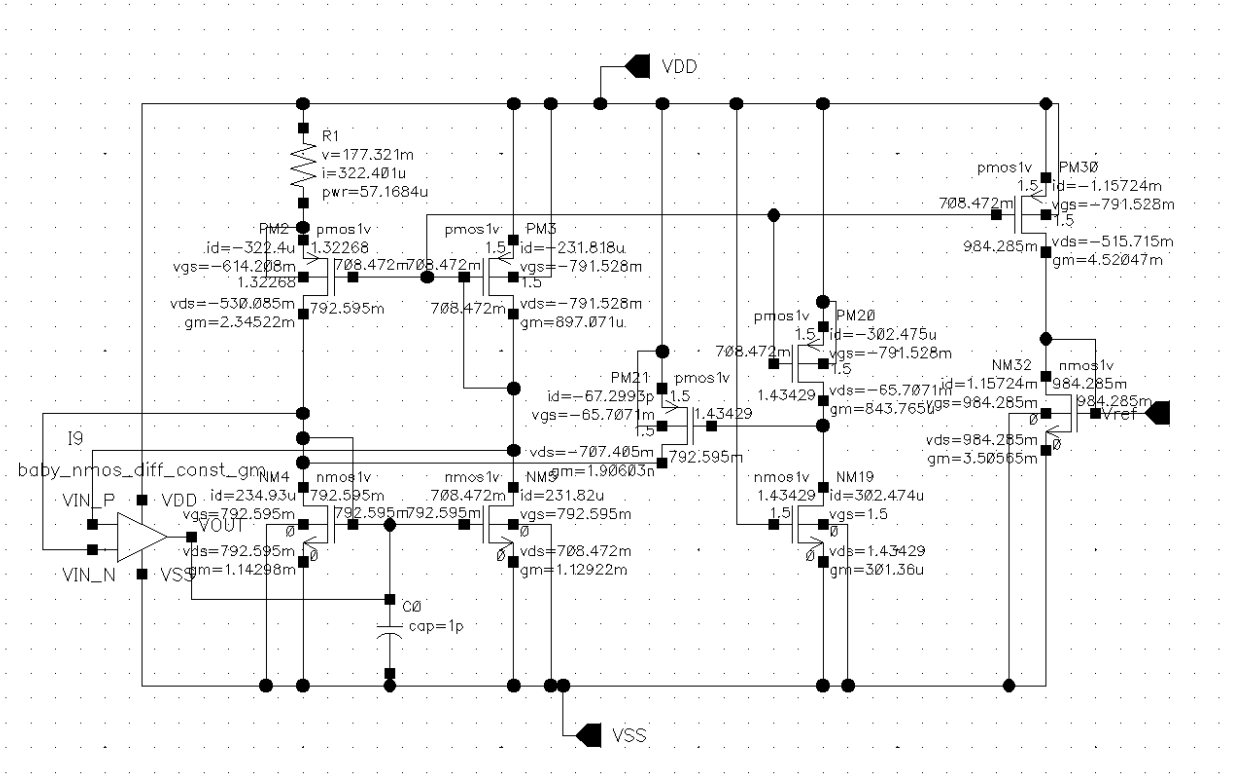

Figure 18: Constant-g_m Bias Circuit for the fully differential OTA

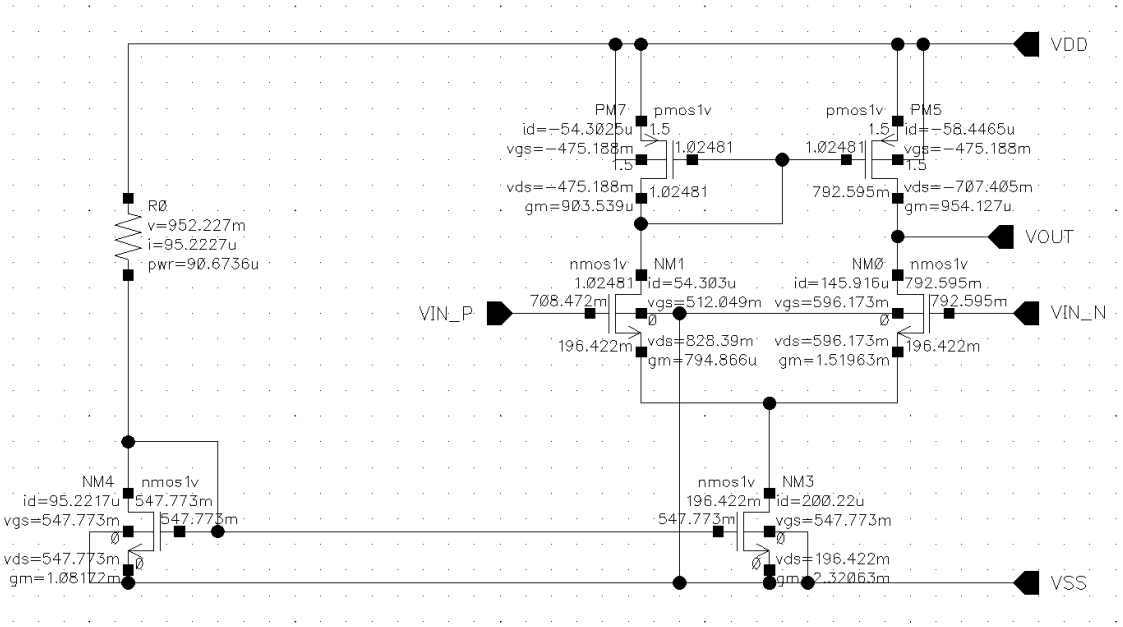

Figure 19: Baby NMOS Differential Amplifier for the Constant-g_m Bias Circuit

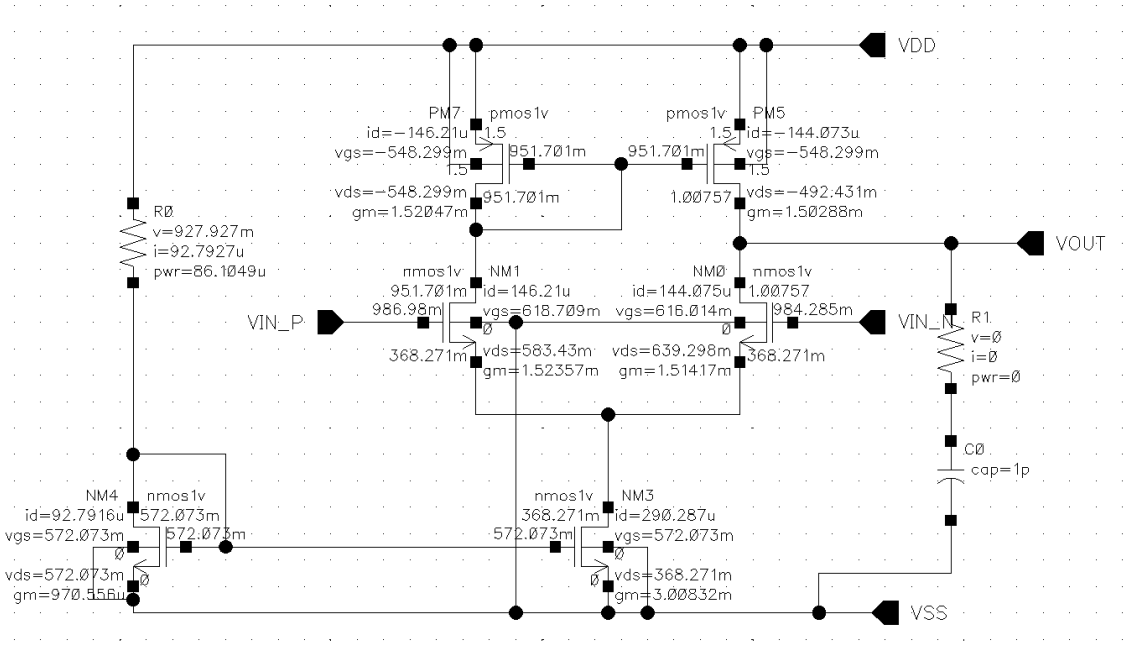

Figure 20: Baby NMOS Differential Amplifier for the common mode feedback of the OTA core.

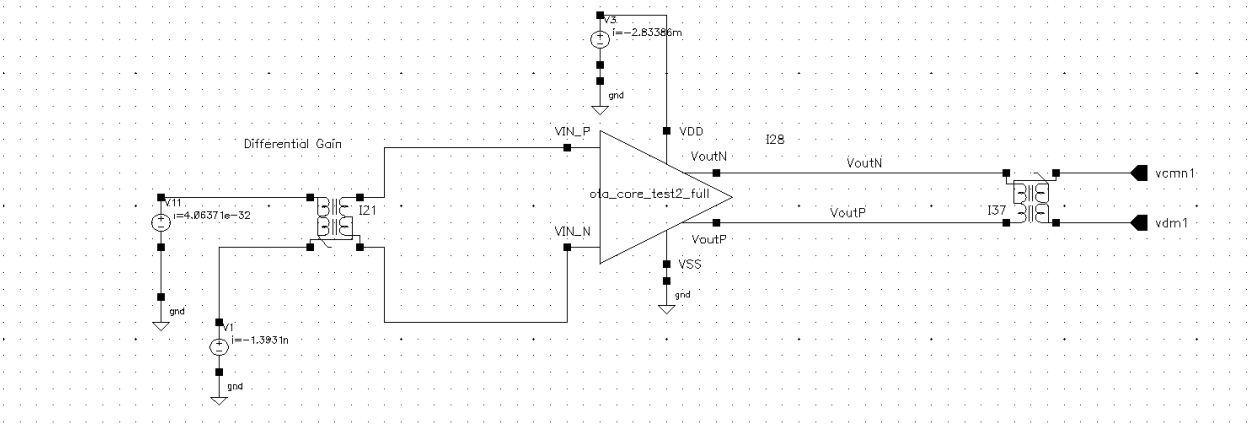

Figure 21: Test bench schematic with DC biasing for evaluating the differential-mode gain using a tail current of 2.83 mA. With a 1.5 V supply, this corresponds to a power dissipation of approximately 4.2 mW.

B Single-Ended Output Folded-Cascode Associated Schematics (Design Values)

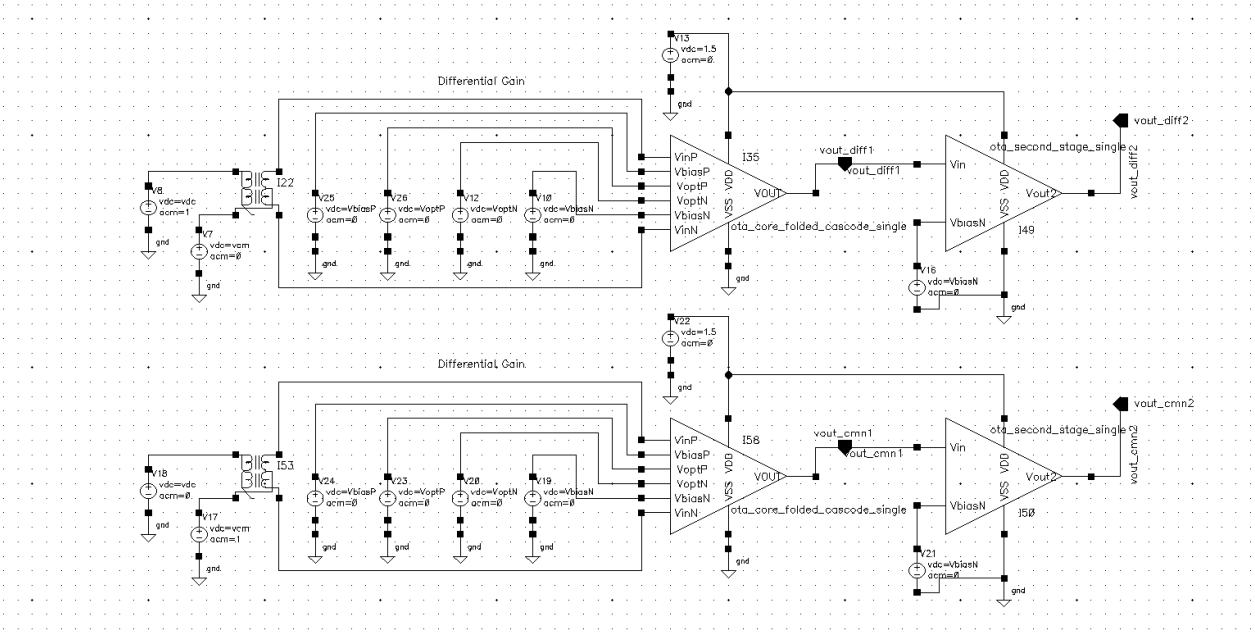

Figure 22: Test Bench schematic with DC biasing for evaluating Common Mode and Differential Mode Gains for the single-ended Folded Cascode Circuit with Second Stage.

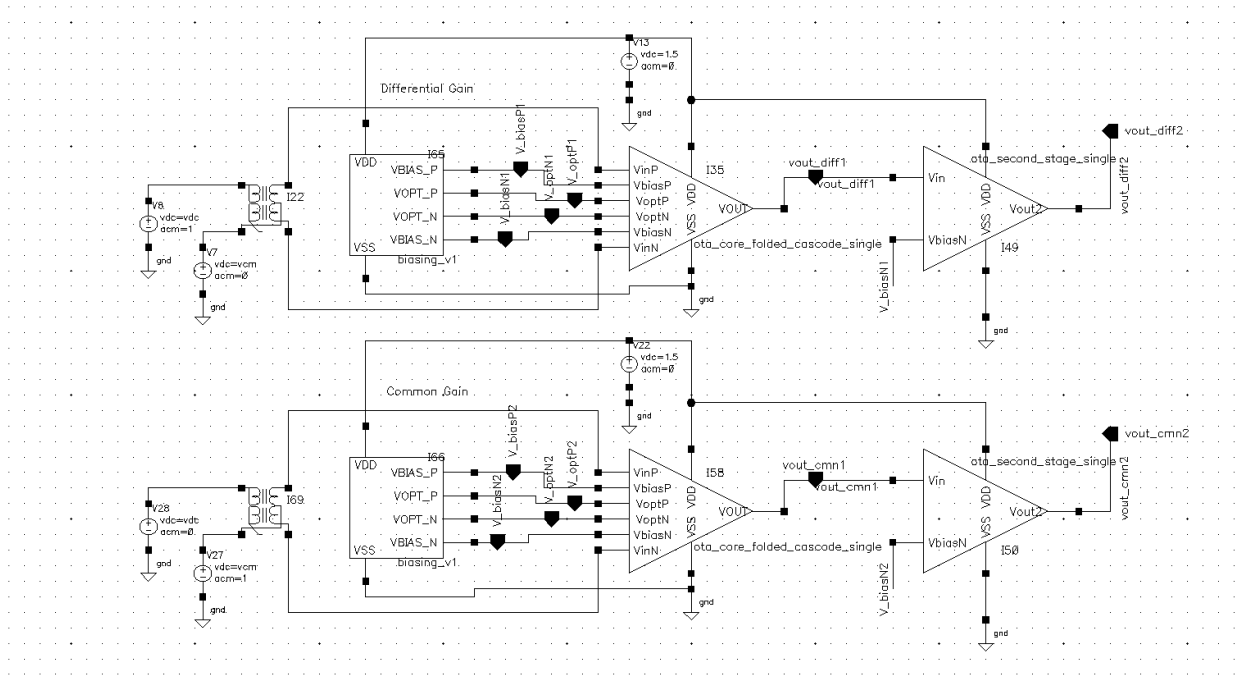

Figure 23: Test Bench schematic with Constant-g_m Bias Circuit for evaluating Common Mode and Differential Mode Gains for the single-ended Folded Cascode Circuit with Second Stage. Note: DC biasing was used for this supplementary circuit with $V_{\text{biasN}} = 0.6$ V, $V_{\text{biasP}} = 1$ V, $V_{\text{optN}} = 1.05$ V, and $V_{\text{optP}} = 0.3$ V.

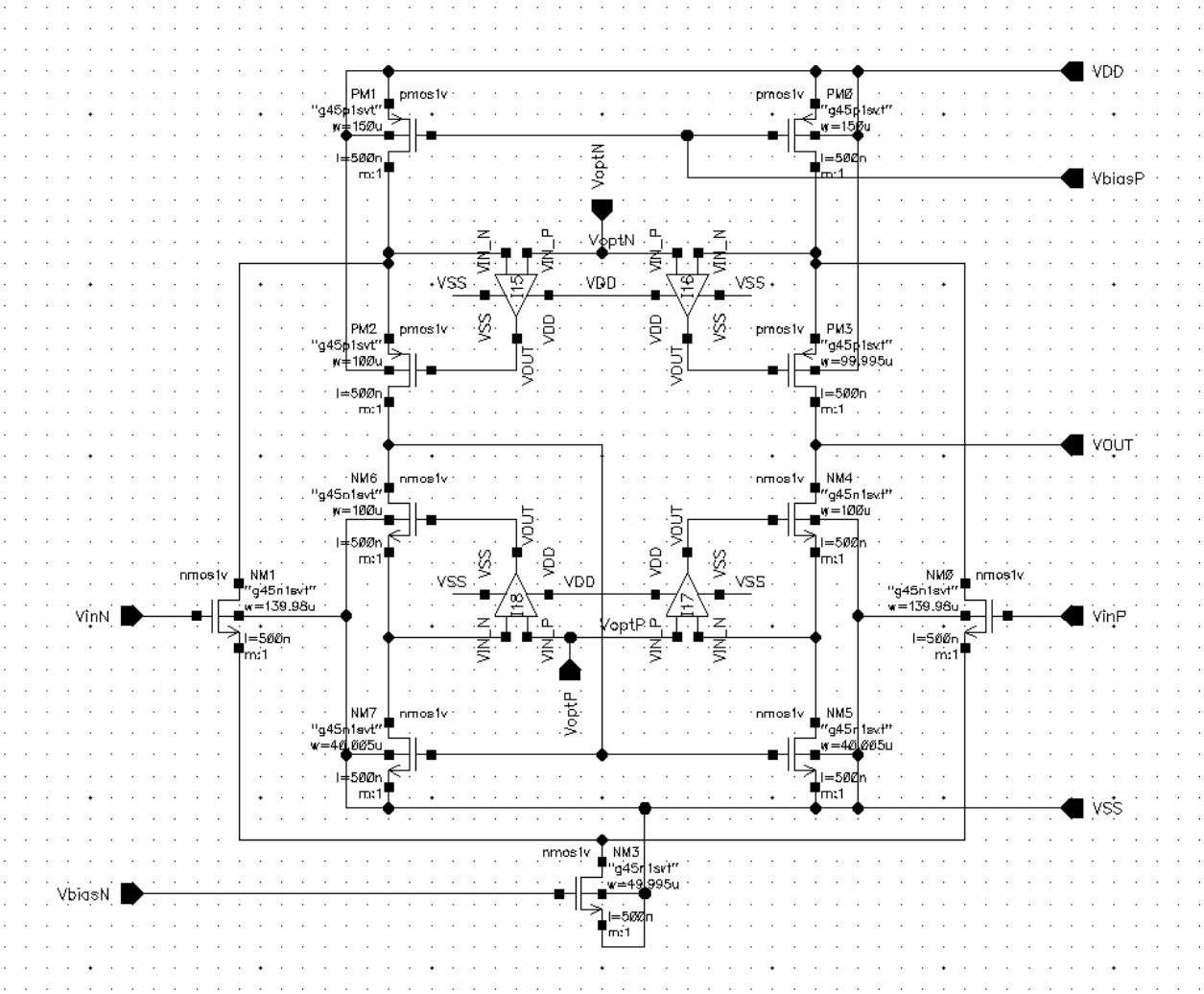

Figure 24: Single-ended core of the OTA folded cascode with baby op-amps

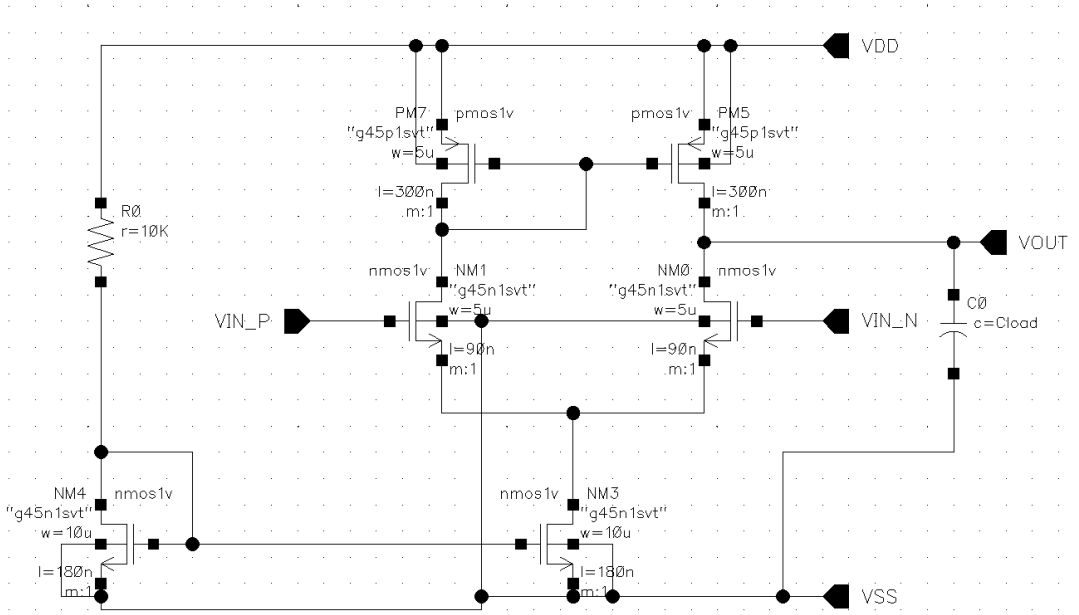

Figure 25: Baby NMOS differential Auxiliary Amplifier for the Folded-Cascode. Cap value undetermined from parameterized sweep.

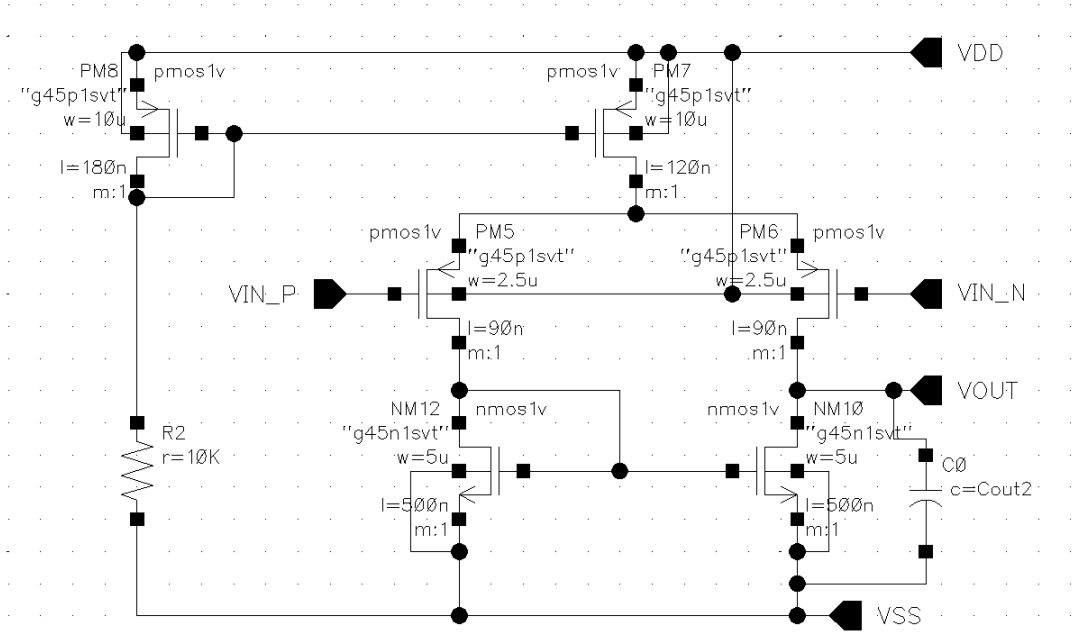

Figure 26: Baby PMOS differential Auxiliary Amplifier for the Folded-Cascode. Cap value undetermined from parameterized sweep.

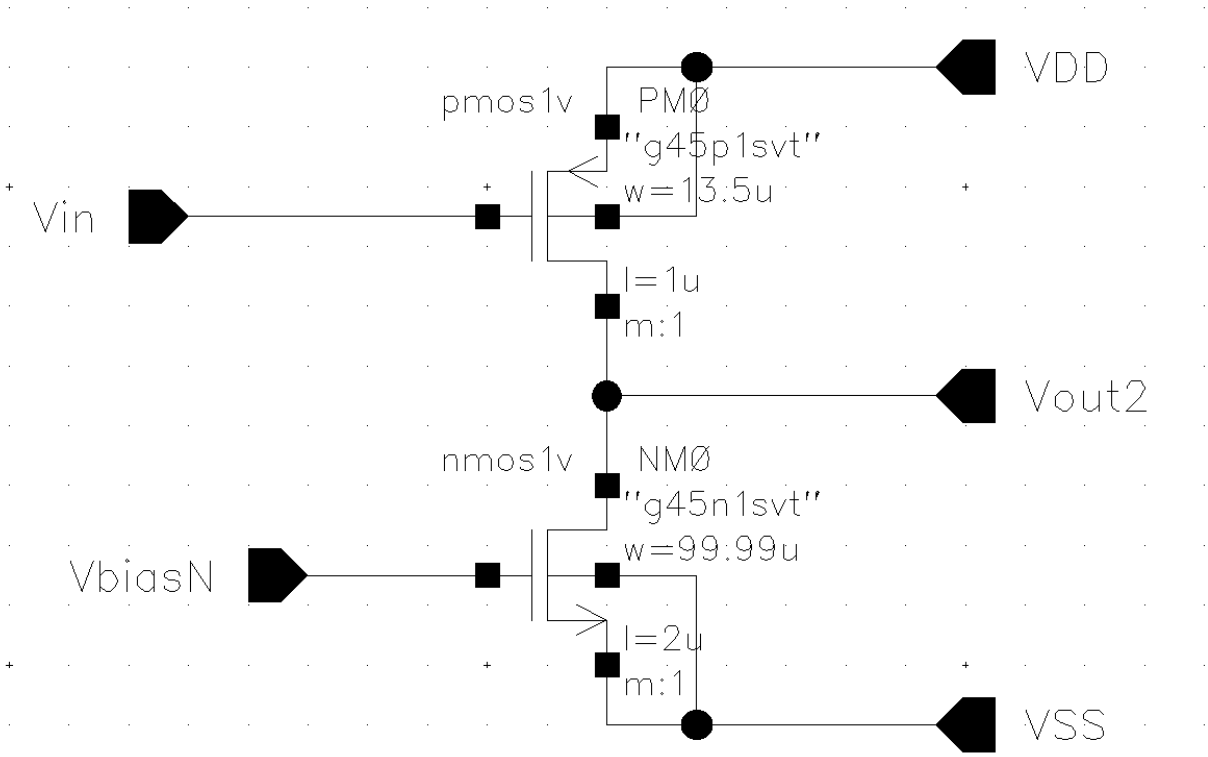

Figure 27: Second-stage PMOS common-source with NMOS load for the Folded-Cascode

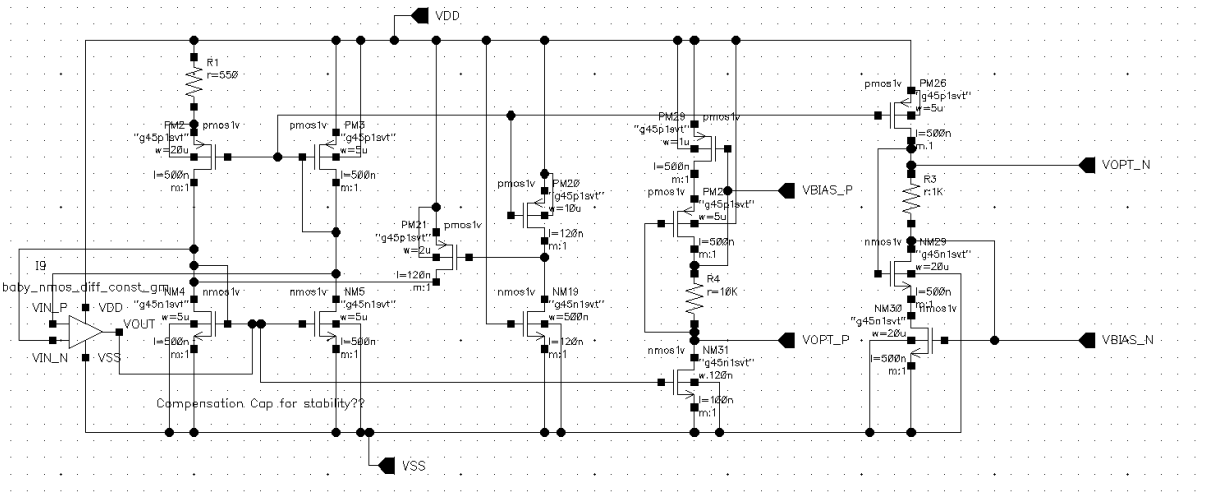

Figure 28: Constant-g_m Bias Circuit for the Folded-Cascode OTA

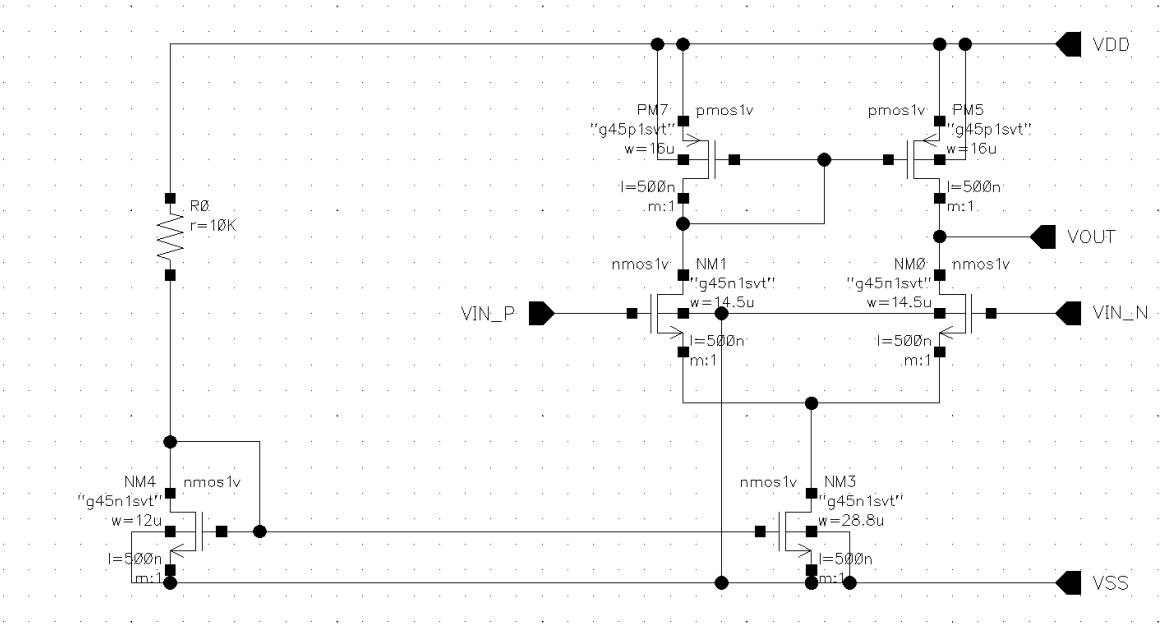

Figure 29: Baby NMOS Differential Amplifier for the Constant-g_m Bias Circuit

C Folded-Cascode Simulation Results

C.1 Single-Ended Output Folded-Cascode Frequency Response

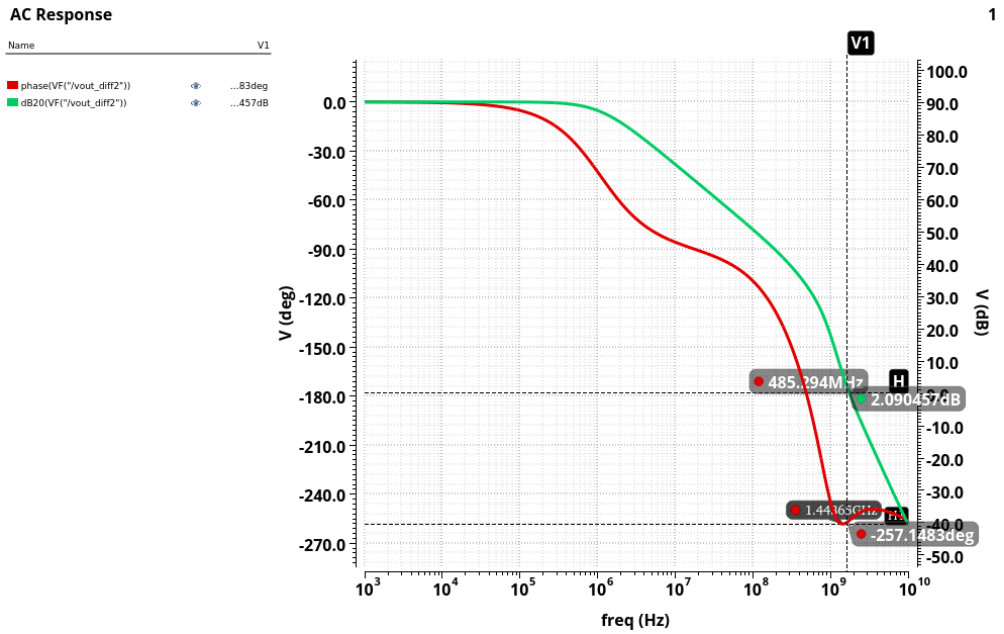

Figure 30: AC response showing gain, bandwidth, and phase margin. As a last minute simulation, frequency compensation was not performed and it is known that this is the incorrect phase margin. Note: DC Biasing was used for the simulation of this supplementary circuit to display our effort on the project where VbiasN = 0.6, VbiasP = 1, VoptN = 1.05, and VoptP = 0.3

C.2 Step Response / Settling Time

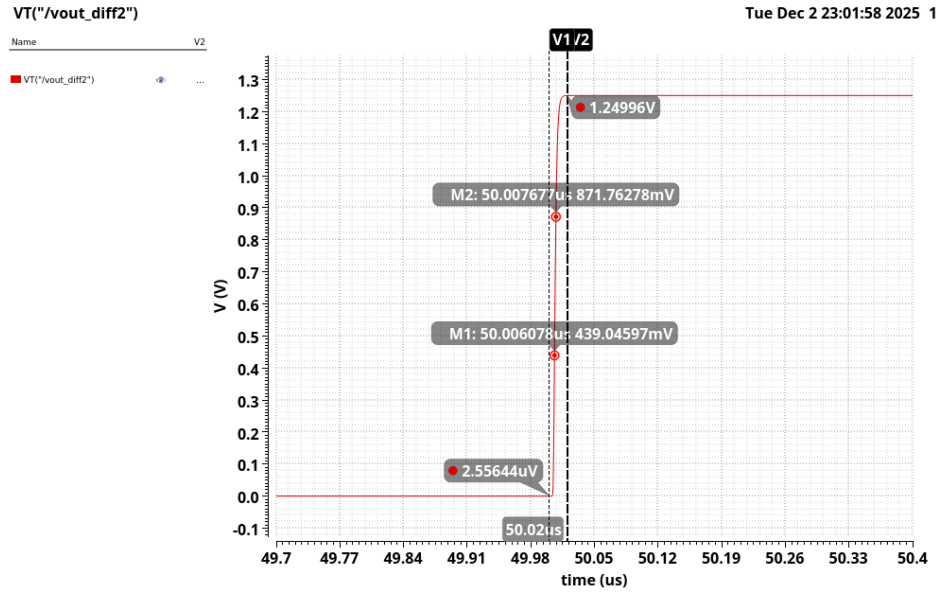

Figure 31: The slew rate(the slope) is roughly 271 V/µs. The settling time is roughly. Note: DC biasing was used for this supplementary circuit with $V_{\text{biasN}} = 0.6$ V, $V_{\text{biasP}} = 1$ V, $V_{\text{optN}} = 1.05$ V, and $V_{\text{optP}} = 0.3$ V.

C.3 DC Input Range

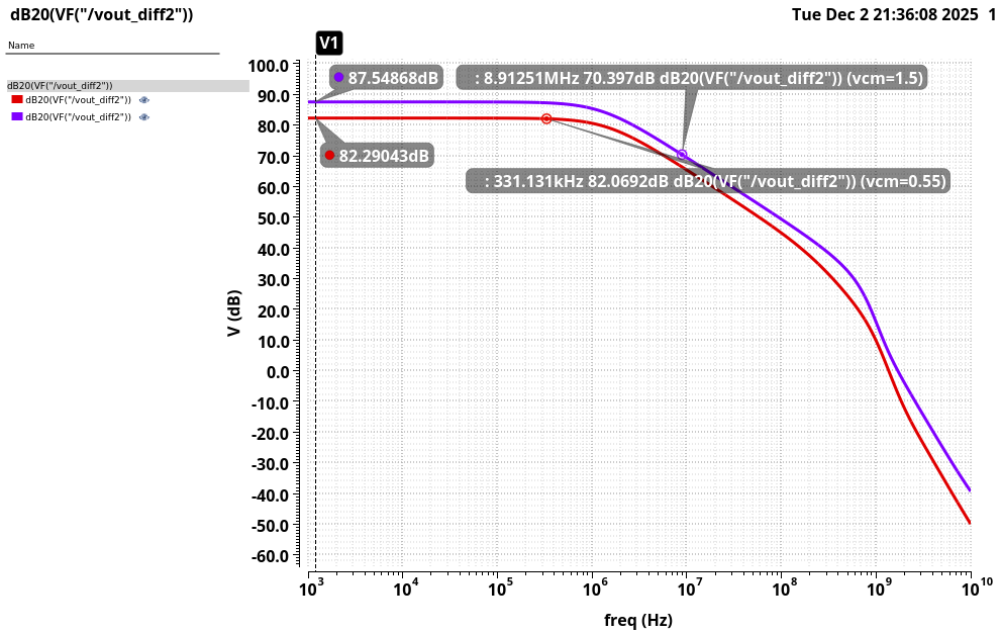

Figure 32: Input Common mode range with Vcm. There is approximately a 6dB difference between vcm = 1.5V and vcm = 0.55v, resulting in 0.95V total range. Note: DC biasing was used for this supplementary circuit with $V_{\text{biasN}} = 0.6$ V, $V_{\text{biasP}} = 1$ V, $V_{\text{optN}} = 1.05$ V, and $V_{\text{optP}} = 0.3$ V.

C.4 Output Range

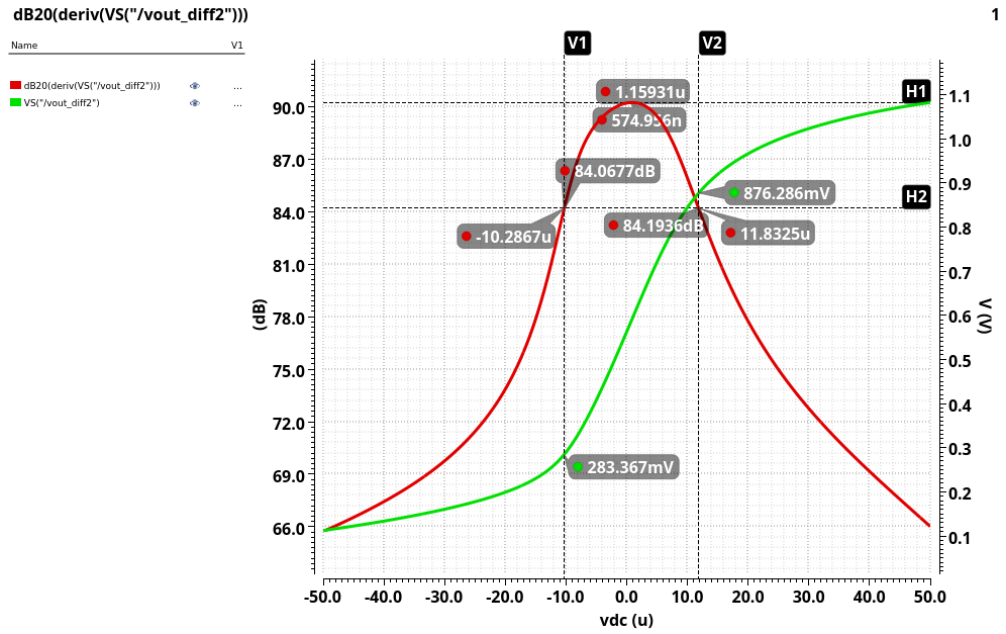

Figure 33: Output Swing Range. There is approximately a total output range of 876mV - 283mV = 593 mV. Note: DC biasing was used for this supplementary circuit with $V_{\text{biasN}} = 0.6$ V, $V_{\text{biasP}} = 1$ V, $V_{\text{optN}} = 1.05$ V, and $V_{\text{optP}} = 0.3$ V.

C.5 CMRR

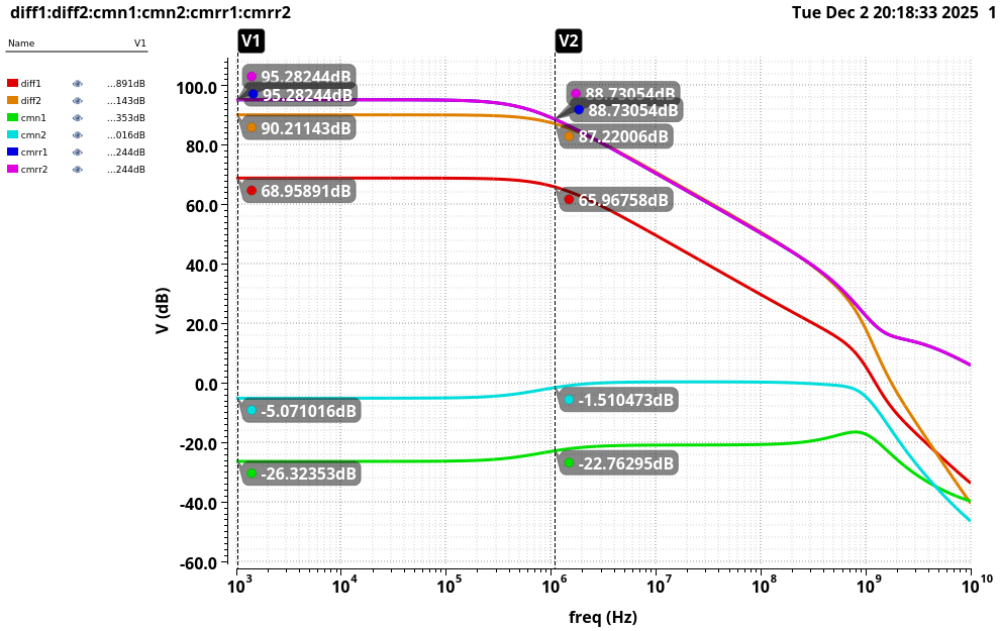

Figure 34: At low frequencies for the second stage output, the CMRR is roughly 95 dB, differential gain is roughly 90.2 dB, and common mode gain is -5 dB. The bandwidth of the circuit after stage 2 is roughly 1MHz. Note: DC biasing was used for this supplementary circuit with $V_{\text{biasN}} = 0.6$ V, $V_{\text{biasP}} = 1$ V, $V_{\text{optN}} = 1.05$ V, and $V_{\text{optP}} = 0.3$ V.

C.6 PSRR+

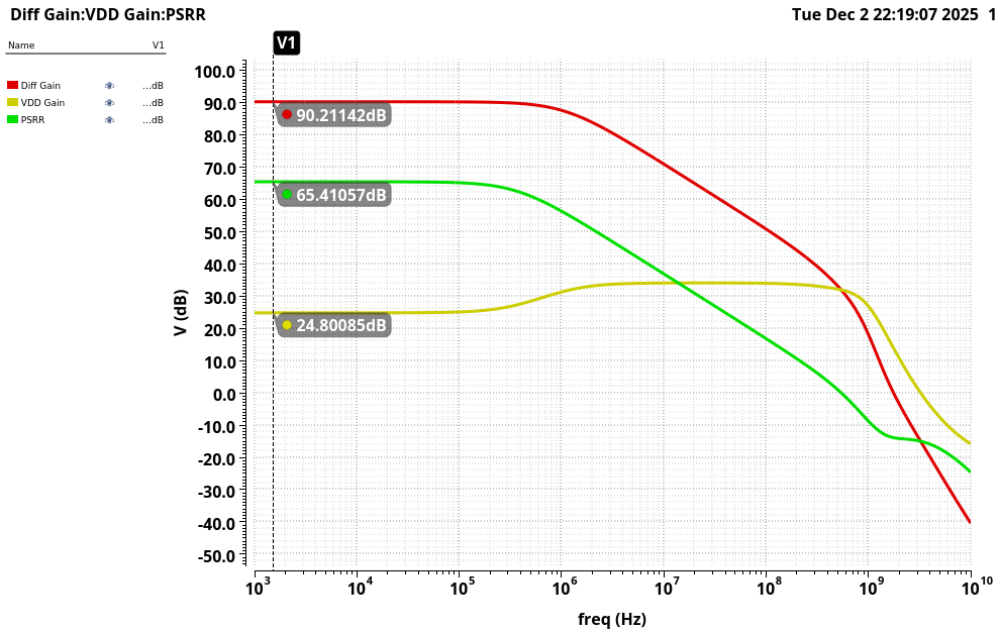

Figure 35: At low frequencies the PSRR is roughly 65 dB. Note: DC biasing was used for this supplementary circuit with $V_{\text{biasN}} = 0.6$ V, $V_{\text{biasP}} = 1$ V, $V_{\text{optN}} = 1.05$ V, and $V_{\text{optP}} = 0.3$ V.

C.7 Input-Referred Noise

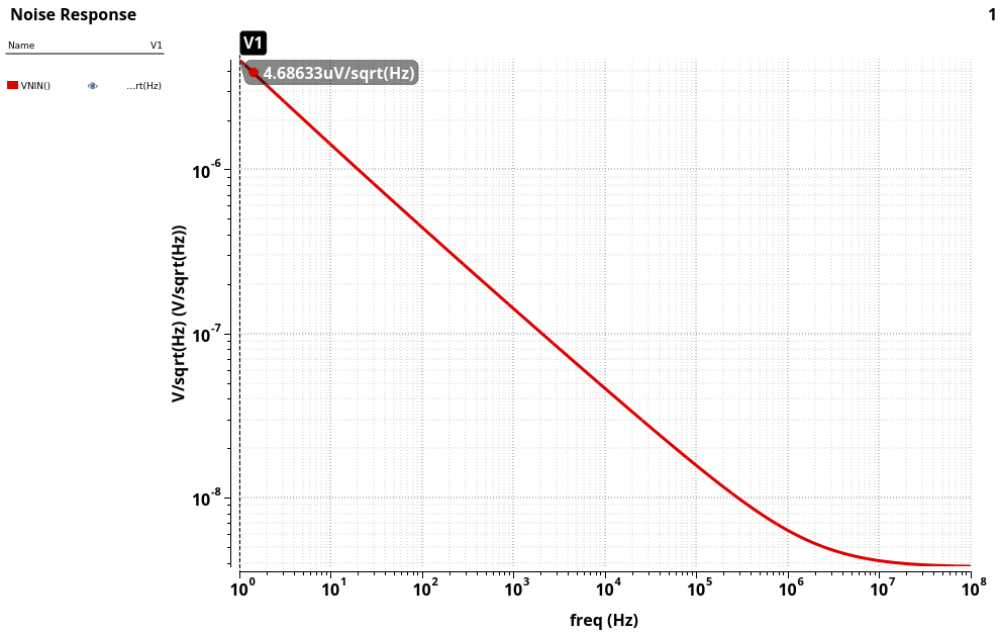

Figure 36: At low frequencies the input-referred noise is roughly 4.68 uV/sqrt(Hz). Note: DC biasing was used for this supplementary circuit with $V_{\text{biasN}} = 0.6$ V, $V_{\text{biasP}} = 1$ V, $V_{\text{optN}} = 1.05$ V, and $V_{\text{optP}} = 0.3$ V.

C.8 Input-Referred Noise

Device	Param	Noise Contribution	% Of Total
I35.PM0.xrg.r1	thermal_noise	0.022713	0.27
I35.PM1.xrg.r1	thermal_noise	0.0227007	0.27
I35.NM0.xrg.r1	thermal_noise	0.0147316	0.11
I35.NM1.xrg.r1	thermal_noise	0.0147313	0.11
I35.NM5.xrg.r1	thermal_noise	0.0134453	0.09
I35.NM7.xrg.r1	thermal_noise	0.0134376	0.09
I35.I16.NM1.xrg.r1	thermal_noise	0.00428083	0.01
I35.I15.NM1.xrg.r1	thermal_noise	0.0042795	0.01
I35.I16.NM0.xrg.r1	thermal_noise	0.00395737	0.01
I35.I15.NM0.xrg.r1	thermal_noise	0.00395636	0.01
I35.I16.PM5.xrg.r1	thermal_noise	0.00223694	0.00
I35.I15.PM5.xrg.r1	thermal_noise	0.00223626	0.00
I35.I16.PM7.xrg.r1	thermal_noise	0.00207589	0.00
I35.I15.PM7.xrg.r1	thermal_noise	0.00207526	0.00
I35.I17.PM5.xrg.r1	thermal_noise	0.00182471	0.00
I35.I18.PM5.xrg.r1	thermal_noise	0.00182361	0.00
I35.I17.PM6.xrg.r1	thermal_noise	0.00167789	0.00
I35.I18.PM6.xrg.r1	thermal_noise	0.00167662	0.00
I35.I17.NM10.xrg.r1	thermal_noise	0.000990346	0.00
I35.I18.NM10.xrg.r1	thermal_noise	0.00098974	0.00

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.439242
Total Input Referred Noise = 4.15753e-05
The above noise summary info is for noise data

Figure 37: Numeric noise results for input-referred noise test. Note: DC biasing was used for this supplementary circuit with $V_{\text{biasN}} = 0.6$ V, $V_{\text{biasP}} = 1$ V, $V_{\text{optN}} = 1.05$ V, and $V_{\text{optP}} = 0.3$ V.